

Chapter 8

Exercise 8.1: A minimum clock width of 5 ns and a latch delay of 2 ns are considered in this problem.

(a) The minimum delay of the combinational network (t_p) considered in this problem is obtained by the following equation

$$t_p + 2ns \geq 5ns \rightarrow t_p \geq 3ns$$

(b) If the delay of the combinational network can decrease by 30% and the latch delay can decrease by 10%, the maximum clock pulse width (T_{max}) is calculated by the following equation:

$$0.7t_p + 0.9 \times 2ns = 0.7 \times 3 + 1.8 = T_{max} \rightarrow T_{max} = 3.9ns$$

Exercise 8.2:

Using the notation given on Figure 8.15 of the textbook we obtain the following network parameters:

Combinational Networks' delays:

$$\begin{aligned} d1_x &= d1_y = 4 * t_p(\text{gate}) = 2ns \\ d2 &= 1 * t_p(\text{gate}) = 0.5ns \end{aligned}$$

Network set-up time:

$$t_{su}^x(\text{net}) = t_{su}^y(\text{net}) = t_{su}(\text{cell}) + d1_x = 1 + 2 = 3ns$$

Network hold time:

$$t_h(\text{net}) = t_h(\text{cell}) = 0.5ns$$

Network propagation delay:

$$t_p(\text{net}) = t_p(\text{cell}) + d2 = 3 + 0.5 = 3.5ns$$

Minimal period:

$$T_{\min} = \max[(t_{in} + t_{su}^x(\text{net})), (t_{su}^y(\text{net}) + t_p(\text{cell})), t_p(\text{net} + t_{out})] = \max[2 + 3, 3 + 3, 3.5 + 2.5] = 6.0ns$$

Maximal frequency:

$$f_{\max} = \frac{1}{T_{\min}} = \frac{1}{6.0 \times 10^{-9}} \approx 167\text{MHz}$$

Exercise 8.3

(a) There are no races because of the nonoverlapping nature of the two clocks. This assures that in each clock cycle only one state change occurs.

(b) The number of states depends on the mode of operation of the network. We consider two modes.

Exercise 8.4

The transition and output functions are described by the following expressions:

$$Y_1 = x'_0 x_1 + x_0 y_1$$

$$Y_0 = y_0 x'_0 + x_0 y_1$$

$$z = y_0$$

PS $y_1 y_0$	Input ($x_1 x_0$)				
	00	01	10	11	
00	00	00	10	00	0
01	01	00	11	00	1
10	00	11	10	11	0
11	01	11	11	11	1
NS($Y_1 Y_0$)					Output (z)

The corresponding state table is (for state assignments $A = 00, B = 01, C = 10, D = 11$ and input coding $a = 00, b = 01, c = 10, d = 11$)

PS	Inputs				
	$x = a$	$x = b$	$x = c$	$x = d$	
A	A	A	C	A	0
B	B	A	D	A	1
C	A	D	C	D	0
D	B	D	D	D	1
NS					Output (z)

The diagram in Figure 8.2 shows the state transitions of this system. The following patterns are recognized by the system (assuming that A is the initial state): cb, cbb, cbc, cd, cdc .

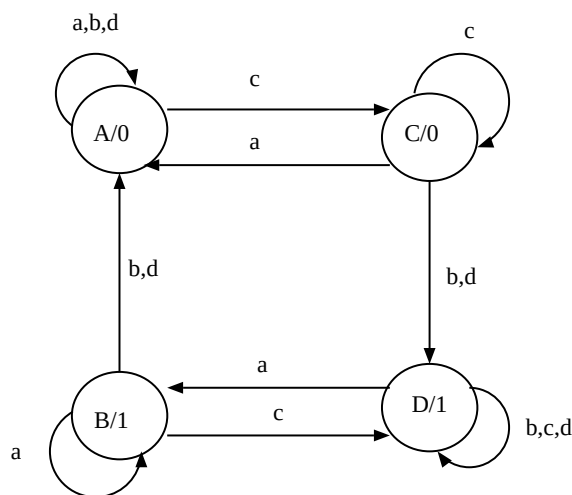


Figure 8.2: State diagram for network on Exercise 8.4

Exercise 8.16 From the network we obtain the following table, based on the expressions below:

$$J_A = K_A = xQ_B$$

$$J_B = K_B = x$$

PS Q_AQ_B	Input		Input	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
00	0000	0011	00	01
01	0000	1111	01	10
10	0000	0011	10	11
11	0000	1111	11	00
	$J_AK_AJ_BK_B$		NS	

The outputs are expressed as:

$$z_3 = Q_AQ_B$$

$$z_2 = Q_AQ'_B$$

$$z_1 = Q'_AQ_B$$

$$z_0 = Q'_AQ'_B$$

Giving the following names to the states:

State Name	Code
S_0	00
S_1	01
S_2	10
S_3	11

we get the transition table:

PS Q_AQ_B	Input		Output
	$x = 0$	$x = 1$	
S_0	S_0	S_1	0
S_1	S_1	S_2	1
S_2	S_2	S_3	2
S_3	S_3	S_0	3
	NS		

The state diagram for the given network is presented in Figure 8.19, and corresponds to a modulo-4 counter with decoded output.

Exercise 8.17

The expression for the flip-flop inputs are

$$J_A = xQ_C \quad J_B = Q'_A \quad J_C = xQ_B$$

$$K_A = xQ'_B \quad K_B = Q_A \quad K_C = x'Q'_B$$

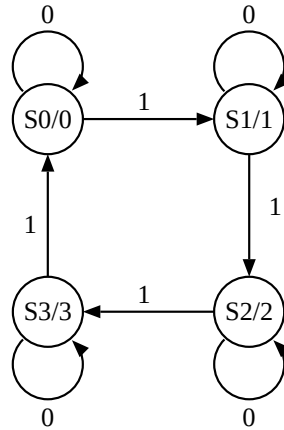


Figure 8.19: State diagram for Exercise 8.16

From the characteristic expressions of the JK flip-flop we get the following expressions for the transition functions:

$$\begin{aligned}
 Q_A(t+1) &= Q_A(t)(x' + Q_B(t)) + xQ'_A(t)Q_C(t) \\
 Q_B(t+1) &= Q_B(t)Q'_A(t) + Q'_B(t)Q'_A(t) \\
 Q_C(t+1) &= Q_C(t)(Q_B(t) + x) + Q'_C(t)xQ_B(t) \\
 z &= Q'_C(t)
 \end{aligned}$$

The corresponding transition table is

PS $Q_A Q_B Q_C$	Input		Input		Output z
	$x = 0$	$x = 1$	$x = 0$	$x = 1$	
000	00,10,01	01,10,00	010	010	1
001	00,10,01	11,10,00	010	111	0
010	00,10,00	00,10,10	010	011	1
011	00,10,00	10,10,10	011	111	0
100	00,01,01	01,01,00	100	000	1
101	00,01,01	11,01,00	100	001	0
110	00,01,00	00,01,10	100	101	1
111	00,01,00	10,01,10	101	101	0
$J_A K_A, J_B K_B, J_C K_C$			NS		

To get a high-level description we define the following code:

$Q_A Q_B Q_C$	state
000	S_0
001	S_1
010	S_2
011	S_3
100	S_4
101	S_5
110	S_6
111	S_7

The resulting state table is

PS	Input		Output
	$x = 0$	$x = 1$	z
S_0	S_2	S_2	1
S_1	S_2	S_7	0
S_2	S_2	S_3	1
S_3	S_3	S_7	0
S_4	S_4	S_0	1
S_5	S_4	S_1	0
S_6	S_4	S_5	1
S_7	S_5	S_5	0
	NS		

The state diagram is shown in Figure 8.20.

A timing diagram can be obtained from the following input/output sequence pairs (the input is arbitrary):

$x(t)$	0	1	0	1	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1	
$s(t)$	0	2	3	3	7	5	4	4	0	2	3	7	5	4	0	2	2	2	3	7
z	1	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	0	1

Exercise 8.18

The expressions for the flip-flop inputs are

$$T_A = Q_A + Q'_B$$

$$T_B = Q_A + Q_B$$

The flip-flops change state in every clock pulse depending only on the previous state. The transition table is

PS	FF inputs		NS
$Q_A(t)Q_B(t)$	$T_A(t)$	$T_B(t)$	$Q_A(t+1)Q_B(t+1)$
00	1	0	10
01	0	1	00
10	1	1	01
11	1	1	00

Let us define the following encoding:

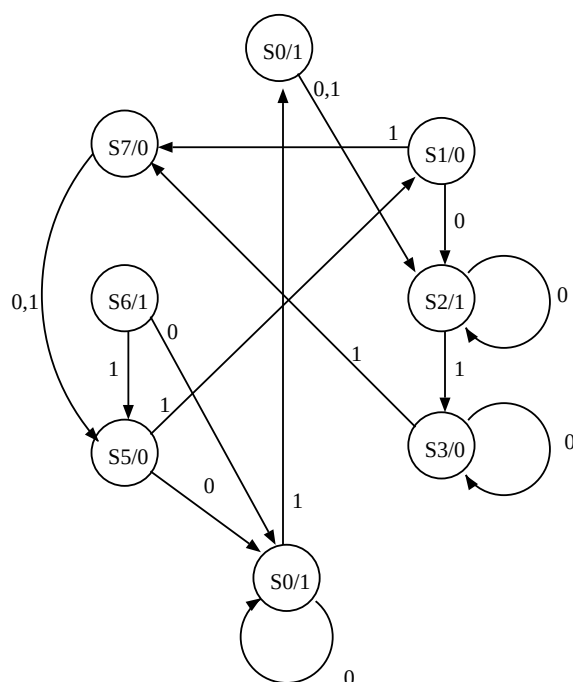


Figure 8.20: State diagram for Exercise 8.17

$Q_A Q_B$	
00	S_0
01	S_2
10	S_1
11	S_3

The resulting state table is

PS	NS
S_0	S_1
S_1	S_2
S_2	S_0
S_3	S_0

The state diagram is presented in Figure 8.21. It is an autonomous modulo-3 counter.

Exercise 8.19

The expressions for the flip-flop inputs and for the output are

$$\begin{aligned}
 J_A &= 1 & K_A &= 1 \\
 J_B &= Q'_C & K_B &= 1 \\
 J_C &= Q_B & K_C &= 1 \\
 z &= Q'_A Q'_B Q'_C
 \end{aligned}$$

The sequential network does not have any input; therefore, the state register changes in each clock pulse depending only on the previous state. The transition table is

$x_3x_2x_1x_0$	$z_3z_2z_0$
0000	0011
0001	0100
0010	0101
0011	0110
0100	0111
0101	1000
0110	1001
0111	1010
1000	1011
1001	1100

This corresponds to the desired converter. A timing diagram is

x	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0
State	S_0	S_1	S_2	S_3	S_0	S_1	S_2	S_3	S_0	S_4	S_5	S_3	S_0	S_4	S_5	S_3
z	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	0

Exercise 8.22

Since the excitation function of a D flip-flop is

$$D(t) = Q(t + 1)$$

the D input for each flip-flop implementation corresponds to its characteristic function. That is,

for a SR flip-flop

$$D(t) = Q(t + 1) = S + R'Q(t)$$

for a T flip-flop

$$D(t) = Q(t + 1) = T \oplus Q(t)$$

for a JK flip-flop

$$D(t) = Q(t + 1) = Q(t)K' + Q(t)'J$$

The corresponding networks are shown in Figures 8.25.

Exercise 8.23

To recognize a sequence with two consecutive 1's followed by one 0 we need to distinguish between the following cases:

$$\begin{aligned} S_2 : & \quad x(t-2) = x(t-1) = 1 \\ S_1 : & \quad \text{Not } S_2 \text{ and } x(t-1) = 1 \\ S_0 : & \quad \text{None of the above} \end{aligned}$$

The corresponding state table is