

CSE 144 (Section Id: 420441)
Computer-Aided Design of VLSI Circuits

Professor Alex Orailoğlu
4840 *AP&M'*
Tel: 858-534-0914 Fax: 858-534-7029
email: alex@cs.ucsd.edu

Course Contents

Introduction The VLSI Design Process. Layout Styles. Challenges in Physical Design.

Partitioning Cost Functions and Constraints. Kernighan-Lin algorithm. Fiduccia-Mattheyses heuristic. Simulated Annealing.

Placement Cost Functions and Constraints. Partition-based methods. Simulated Annealing. Force-Directed Placement.

Grid Routing Cost Functions and Constraints. Maze Routing Algorithms. Line Search Algorithms. Multilayer Routing. Net ordering. Rip-up and rerouting.

Channel Routing Cost Functions and Constraints. Constraint Graphs. Left-edge algorithm. Dogleg algorithm. Yoshimura and Kuh algorithm. Greedy channel router. Switchbox routing.

Layout Generation Standard Cell Generation. Optimization of Gate-Matrix Layout. Programmable Logic Arrays. PLA Logic Synthesis. PLA Folding.

Silicon Compilation Time-Constrained Scheduling. Allocation Tasks. Functional Unit Binding. Storage Unit Binding. Interconnection Binding.