Statistical Compact Modeling and Si Verification Methodology

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Abstract
As we scale down to sub-65nm technologies, transistors and interconnects no longer act as predictable elements, but start acting as statistical blocks due to static and dynamic variations. This invited talk first reviews some of the key variations that need to be considered for any statistical analysis. Also, details for implementing statistical models into compact modeling flow are discussed. Finally, the paper reviews one of the techniques used for generating and validating statistical models with the silicon data.

1. Introduction
With technology scaling, integrated circuits are becoming increasingly vulnerable to different sources of variations. The sources of variations can be broadly classified into two categories [1]. The first set of variations can be grouped under dynamic variations, which arise during the operation of the circuit such as variations in supply voltage, switching activity and die temperature. The other set can be grouped under static variations, which arise during the fabrication. These static variations, which arise due to the process, can either be extrinsic (such as variations in channel length, gate oxide thickness, interconnect width and thickness, inter-metal layer dielectric thickness, contact and via sizes) or intrinsic (such as random fluctuations of dopant atoms in the channel of a MOSFET device).

The dynamic/static variations can be further classified into die-to-die and within-die variations. Die-to-die variations, which result from lot-to-lot, wafer-to-wafer variations, impact each element on the die equally. Contrary to die-to-die variations, within-die variations consisting of both systematic and random components produce non-uniformity of electrical characteristics across the die. In contrast to die-to-die variations, within-die variations contribute to the loss of matched behavior between structures on the same die.

The within die variations can also exhibit spatial correlations, where devices that are close to each other have a higher probability of being alike than the devices that are far apart. Spatial correlations are generally modeled by decomposing within-die variations into two components: systematic and random, where systematic component is a function of spatial position of a device in the die. Apart from analyzing variations for a single device on a die, mismatch between a pair of device are also studied. This kind of mismatch analysis is critical for those pair of transistors, where mismatch can lead to degradation in performance/stability. In general, this mismatch is a strong function of device geometry and distance between the devices.

A comprehensive methodology needs to be developed to generate compact models to capture the impact of parameter variations in the design flow. This paper reviews some of the key variations that need to be considered for any statistical analysis. Also, it reviews techniques used for generating and correlating statistical models with Si. The paper is organized as follows: Section 2 reviews parameters that are widely used to capture the impact of variations. Section 3 discusses our in-house statistical models and also presents some of the results for comparison of our variation wrapper with Si data. Section 4 reviews an existing approach used to correlate statistical models with Si data. Section 5 concludes this paper.

2. Statistical Device and Interconnect Variations
2.1. Device Variations
The device parameters that are known to vary are oxide thickness, channel length, channel width, doping concentration and poly/metal grain structure [1]. Some of these parameters are shown in Figure 1.1 below.

![Figure 1.1: Schematic of an N-channel MOSFET. Varying parameters are channel length (L), channel width (W) (not shown), oxide thickness (t_{ox}), doping concentration (N_{ch}), metal gate/poly gate microstructure (not shown) [2].](image)

Oxide thickness is a critical parameter; however, it is well controlled. Length and width variations typically arise because of the optical proximity effects or...
mask/lens/photo system deviations or due to plasma etch dependencies. Out of these variations, channel length variations are considered the most dominant because of its considerable impact on output current characteristics.

Apart from variations in channel length, dopant fluctuations can arise due to variation in implant dose, energy or angle and it can result in variation in other electrical parameters such as threshold voltage [3]-[4]. Figure 1.2 below shows a schematic diagram for a MOSFET, and also depicts the surface conduction band edge due to uniformly placed channel dopants (top left) and randomly placed (Poisson distributed) channel dopants (top right). In the random dopant case, the potential fluctuations cause hills and valleys in the barrier affecting threshold voltage and subthreshold current flow from the source to drain. With miniaturization of CMOS circuits, it has been shown that the number of dopant atoms in the channel region scales rapidly (Figure 1.3) [5].

Figure 1.2: Surface conduction band edge under uniform and non-uniform distribution of channel dopants [2].

Figure 1.3: Mean number of dopant atoms at various technology nodes. With technology scaling, number of dopant atoms scale rapidly, thus posing a major challenge for future nanoscale designs [6].

Due to relatively small number of dopant atoms at more advanced technology nodes, even small variations in dopant density and dopant placement can pose a major challenge for future nanoscale designs. Because of their intrinsic nature, dopant fluctuations are much more difficult to control as compared to extrinsic variations such as variations in channel length etc. These variations in dopant concentration and placement are often studied by focusing on electrical parameters such as threshold voltage which is directly extracted and modeled.

The effects of channel length and width, oxide thickness, and doping concentration on random dopant induced threshold voltage lowering and fluctuations are studied in [4]. It was concluded that both threshold voltage lowering as well as fluctuations increase with increase in doping level and the oxide thickness and with the decrease in channel length. The threshold voltage fluctuation decreases and threshold voltage lowering increases with the increase of channel width.

Apart from analyzing variations for a single device on a die, mismatch between a pair of devices is also studied. As discussed earlier, the variations can have systematic as well as random components. It becomes increasingly important to differentiate between random and systematic components while analyzing mismatch between devices. Since mismatch refers to the differential performance of two or more devices in adjacent placement, different scenarios for mismatch can arise. For instance, if the variations for the devices are assumed to be completely random, then the variance for the mismatch will be twice the variance of the individual device. These random components of mismatch are generally inversely proportional to device area, thus increasing the size of structure would result in better matching between the devices. On the other hand, when the variations are not completely random and have significant systematic components, it would result in a lower variance for mismatch between the devices. These systematic components of mismatch are strong functions of distance between the devices. Thus, a good strategy to ensure good matching in this case would be to keep devices as close to each other as possible. Out of all these components, random dopant fluctuations discussed above are found to be the main cause of device mismatch.

2.2. Interconnect Variations

Interconnect variations have their ties all the way down to process parameters. Variations in lithography, reactive ion etch and variations in DHF oxide strip clean can result in variations in interconnect width [7]. Variations in low-k deposition depth [8], hard mask depth, etch and hardmask erosion, sputter depth, polish target and chemical mechanical polishing result in variations in interconnect height. These process variations result in variations in physical interconnect parameters. In a circuit, variations in these physical parameters will change the electrical parameters, such as...
resistances and capacitances. In order to consider the interconnect variations in simulations, when possible, equations should be tied to the process parameters as identified above. As these process parameters are not correlated, the results will be most accurate. If this is not possible or too costly, for example for circuit timing simulations, then the models should incorporate the variations in the physical parameters. At this step, the physical parameters, such as width and height, will likely be correlated, and hence necessary computational methods such as principal component analysis [9] or alternatives [10] should be implemented in order to reduce or eliminate the inaccuracies caused by correlation between parameters.

3. Implementation of Statistical Compact Models

Our in-house statistical model can be represented in the following form (Figure 1.4):

![Figure 1.4: Device level statistical modeling can be done by building a variation wrapper above a model card. Here, the impact of parameter variations is captured in a compact model through a variation wrapper by assuming certain distributions for chosen set of parameters (such as channel length, width and long channel threshold voltage). The model card is generated by applying a standard model extraction methodology, while variation wrapper is generated from measured data collected across different sites in dies/wafers or from different lots. The results for comparison of our variation wrapper with Si data for a matched pull up transistor pair are presented next.](image)

Note that for matched pair of transistors, it is important to match the spread for single transistors as well as the mismatch between them. The results are shown in Figure 1.5 for Vtsat. In the figure, the first row plots the simulated results for pull-up # 1, pull-up # 2 and the difference between the two ((1)-(2)) using Monte Carlo simulations. The second row shows the measured data for the same. In the third row, we plot (1) vs. (2) to match the shape of mismatch cloud. As can be clearly seen from the plots, the variation wrapper captures the spread in the single transistor as well as in a matched pair of transistors.

4. Modeling and Validation with Silicon Data

Here, we review an approach based on propagation of variance (POV) discussed in [11]. We chose this approach since we found it accurate and simple as well as much less time consuming as compared to Monte Carlo simulations. We first briefly review this approach and then check its accuracy against Monte Carlo simulations. The POV relationship is depicted in the Figure 1.6.

![Figure 1.6: Propagation of variance relationship [11] For a given independent variable x, and a dependent variable y = g(x):](image)

\[
\Delta y = \frac{dy}{dx} \Delta x 
\]  

(1)

Considering the range of possible values of \(\Delta x\) as described by the probability density function (pdf) of x and building a pdf (y) yields the POV relationship:

\[
\sigma_e^2 = \sum p_i \left(\frac{de}{dp_i}\right)^2 \sigma_{pi}^2 
\]  

(2)

where e is any electrical parameter and \(p_i\) is the ith independent process parameter. So, given approximate variance values for some set of parameters, the resulting first order electrical impact of the variations on device or circuit level can be easily derived.

We validated POV approach by comparing it with direct Monte Carlo (MC) simulations. The results are shown in Table 1. The comparison was done for two parameters: Idsat (uA/um) and Vtsat (V). Sensitivities shown in the table were computed using (1). \(\sigma_e^{POV}\) represents the standard deviation computed using POV approach (2), while \(\sigma_e^{MC}\) represents the standard deviation computed using direct Monte Carlo simulations.
from Monte Carlo simulation. Variation in input parameters \((L, W, V_{th})\) were assumed to be the same in both the cases. As can be clearly seen from Table 1, the results from POV approach match reasonably well with Monte Carlo simulations. However, since Monte Carlo simulations are time consuming, POV approach could be a good alternative for estimating the impact of parameter variations.

### Table 1: Comparison of POV approach with Monte Carlo simulations

<table>
<thead>
<tr>
<th></th>
<th>I_{dsat}</th>
<th>V_{tsat}</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\sigma_{\epsilon}^2)</td>
<td>-2500</td>
<td>-0.5087</td>
</tr>
<tr>
<td>(\sigma_{\epsilon}^2)</td>
<td>1166.7</td>
<td>0.9931</td>
</tr>
<tr>
<td>(\sigma_{\epsilon}^2)</td>
<td>1000</td>
<td>~0</td>
</tr>
<tr>
<td>(\sigma_{\epsilon}^{MC})</td>
<td>29.37</td>
<td>0.0158</td>
</tr>
<tr>
<td>(\sigma_{\epsilon}^{MC})</td>
<td>29.59</td>
<td>0.017</td>
</tr>
</tbody>
</table>

Since results from POV approach match well with Si data, we can use it to back propagate the variances in input parameters. First, we use the measurement data to calculate the deviation in \(L, W\) and \(V_{th}\) for single transistor. The data that could be used for this purpose could be the deviations for \(I_{dsat}, I_{dh}, I_{dl}, V_{tsat}\), and \(V_{lin}\). The data for different transistor sizes and types, \(\sigma_{\epsilon}^{POV}\) (for instance pull down, pass and pull up transistors) can be used. So, for each of the measured parameter and transistor sizes and types, we can write the following:

\[
\sigma_{\epsilon}^2 = \left(\frac{\partial \epsilon}{\partial L}\right)^2 \sigma_L^2 + \left(\frac{\partial \epsilon}{\partial W}\right)^2 \sigma_W^2 + \left(\frac{\partial \epsilon}{\partial V_{th}}\right)^2 \sigma_{V_{th}}^2 \tag{3}
\]

or equivalently,

\[
Y_i = X_{1i} \beta_1 + X_{2i} \beta_2 + X_{3i} \beta_3 \tag{4}
\]

where,

\[
X_{1i} = \frac{\partial \epsilon}{\partial L} \quad X_{2i} = \frac{\partial \epsilon}{\partial W} \quad X_{3i} = \frac{\partial \epsilon}{\partial V_{th}} \tag{5}
\]

\[
\beta_1 = \sigma_L^2 \quad \beta_2 = \sigma_W^2 \quad \beta_3 = \sigma_{V_{th}}^2
\]

\(i=1, 2, ..., n\), where each \(i\) corresponds to one of the different simulation set up. The \(\beta_i's\) can be calculated using linear regression techniques. Similarly, the mismatch numbers for \(L, W\) and \(V_{th}\) can be calculated using the mismatch data. Thus,

\[
\sigma_{\epsilon_{ni}}^2 = 2\left(\left(\frac{\partial \epsilon}{\partial L}\right)^2 \sigma_{\epsilon_{ni}}^2 + \left(\frac{\partial \epsilon}{\partial W}\right)^2 \sigma_{\epsilon_{ni}}^2 + \left(\frac{\partial \epsilon}{\partial V_{th}}\right)^2 \sigma_{\epsilon_{ni}}^2\right) \tag{6}
\]

Linear regression technique can be again applied to calculate the mismatch numbers.

### 5. Conclusion

This work reviewed some of the key device and interconnect variations that need to be considered for any statistical analysis. Specifically for mismatch analysis, fluctuation in dopant concentration was found to be a significant source of variation. We also compared the results from variation wrapper with measured Si data and spread for both single transistor as well as matched pair of transistors matched well with measured Si data. Finally, a key approach based on Propagation of Variance (POV) was discussed for validating the models with Si data which was also validated through direct Monte Carlo simulations.

### References


