Lecture 18:
Sequential Networks: Timing and Retiming

CSE 140: Components and Design Techniques for Digital Systems

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Q1: Consider the following FSM, that has one input x.

If 1 bit (Q) is used to represent the state, what is the assumed state encoding for the given state table:

A. \( S_0: 0, S_1: 1 \)
B. \( S_0: 1, S_1: 0 \)
C. Both of the above are correct
D. Neither is correct

State table:

<table>
<thead>
<tr>
<th>Q\x</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( S_1 )</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>( S_0 )</td>
<td>0</td>
</tr>
</tbody>
</table>
Q2: If a JK flip flop is used to implement the given state table, what is the most reduced expression for \( J(t) \) in terms of the \( Q(t) \) and \( x(t) \)?

A. \( J(t)=1 \)
B. \( J(t)=Q(t) \)
C. \( J(t)=Q(t)' \)
D. \( J(t)=Q(t)x(t) \)
E. Neither is correct
Q3: A unique FSM (diagram) can be obtained from a given sequential circuit for a fixed choice of:

A. Flip-flops (e.g. D, T, JK)
B. State encoding
C. Inputs
D. Outputs
E. None of the above
Q4: Which of the following is the correct state equation for the given sequential circuit?

A. \( Q_1(t) = Q_0(t)' \), \( Q_0(t) = Q_0(t) + Q_1(t) \)
B. \( Q_1(t+1) = Q_0(t)' \), \( Q_0(t+1) = Q_0(t) + Q_1(t) \)
C. \( Q_1(t+1) = Q_1(t)' \), \( Q_0(t+1) = Q_0(t) + Q_1(t) \)
D. None of the above
Q5: If $t_{\text{setup}}$ is the setup time of a flip flop then a “setup time violation” is said to occur for the flip-flop if:

A. The output of the flip flop does not remain stable for at least $t_{\text{setup}}$ time after the rising edge of the clock
B. The output of the flip flop does not remain stable for at least $t_{\text{setup}}$ time before the rising edge of the clock
C. The input to the flip flop does not remain stable for at least $t_{\text{setup}}$ time after the rising edge of the clock
D. The input to the flip flop does not remain stable for at least $t_{\text{setup}}$ time before the rising edge of the clock
Fact 1: Once a flip flop has been ‘built’ we are stuck with its timing characteristics: $t_{\text{setup}}$, $t_{\text{hold}}$, $t_{\text{ccq}}$, $t_{\text{pcq}}$.

Now let’s look at the timing characteristics of the combinational part.
Combinational Logic Timing

I. Min delay of a gate, also called Contamination delay: \( t_{cd} \)
Minimum time from when an input changes until the output \( \text{starts} \) to change

II. Max delay of a gate, also called Propagation delay: \( t_{pd} \)
Maximum time from when an input changes until the output \( \text{is} \) guaranteed to reach its final value (i.e., stop changing)
PI Q: Which path in the above circuit determines the contamination delay of the circuit (assuming the delay of all the gates is the same)?

A. Green path
B. Red path
C. Both
D. Neither
Combinational Logic: Output timing constraints

PI Q: Which path in the above circuit determines the propagation delay of the circuit (assuming the delay of all the gates is the same)?

A. Green path
B. Red path
C. Both
D. Neither

\[ t_{pd\ of\ circuit} = 3 \times t_{pd\ of\ gate} \]
To meet the hold time constraint:

\[ t_{\text{hold}} < \text{min delay(flipflop)} + \text{min delay(combinational)} \]

\[ t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}} \]

Also called: min CLK to Q delay

Contamination delay of R1

If D2 starts changing before Q1 as shown, it would be a hold violation.
To meet the setup time constraint:

\[ T_c \geq \max \text{ delay(flipflop)} + \max \text{ delay(combinational)} + t_{\text{setup}} \]

\[ T_c \geq t_{\text{pcq}} + t_{\text{pd}} + t_{\text{setup}} \]
Timing Analysis

Timing Characteristics

- $t_{ccq} = 30 \text{ ps}$
- $t_{pcq} = 50 \text{ ps}$
- $t_{setup} = 60 \text{ ps}$
- $t_{hold} = 70 \text{ ps}$
- $t_{pd} = 35 \text{ ps}$
- $t_{cd} = 25 \text{ ps}$

Setup time constraint:

$$T_c \geq \left( t_{pcq} + t_{pd} + t_{schw} \right)$$

$$f_c = \frac{1}{T_c} = \left( 50 + 105 + 60 \right)$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{hold} ?$$
Timing Analysis

Timing Characteristics

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$t_{hold} = 70 \text{ ps}$

$t_{pd} = 35 \text{ ps}$

$t_{cd} = 25 \text{ ps}$

Setup time constraint:

$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$

$f_c = \frac{1}{T_c} = 4.65 \text{ GHz}$

Hold time constraint:

$t_{ccq} + t_{cd} > t_{hold}$?

$(30 + 25) \text{ ps} > 70 \text{ ps}$? No!
Fixing Hold Time Violation

Add buffers to the short paths:

Timing Characteristics

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- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps
- $t_{cd} = 25$ ps

Setup time constraint:

$T_c \geq f_c$

Hold time constraint:

$t_{ccq} + t_{pd} > t_{hold}$?
Fixing Hold Time Violation

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Timing Characteristics

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Setup time constraint:
\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]
\[ f_c = 1/T_c = 4.65 \text{ GHz} \]

Hold time constraint:
\[ t_{ccq} + t_{cd} > t_{hold} \]
\[ (30 + 50) \text{ ps} > 70 \text{ ps} \text{ ? Yes!} \]