Lecture 1: Introduction to Digital Logic Design

CSE 140: Components and Design Techniques for Digital Systems
Spring 2014

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Information about the Instructor

- Instructor: CK Cheng
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- Office hours: CSE2130
  - 1:30-2:20PM, T
  - 10:30-11:20AM, Th
Information about the Instructor

• Instructor: Diba Mirza
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• Office hours:
  – M 10:30am- 11:30 am, T 11am –noon
  – Or by appointment
Information about TAs

*TAs shared between sections A and B

- Krithika Singh
- Vineel Pratap Konduru
- Xiao Liu
- Alireza Khodamoradi
- Anup Chenthamarakshan
- Yichi Zhang
- Dao Dinh Lam
- Vidya Kirupanidhi
- Jongchyi Su

Office hours and emails available on the course website
Logistics: Resources

All information about the class is on the class website:
http://cseweb.ucsd.edu/classes/sp14/cse140-b/index.html

- *Approx.* Syllabus
- Detailed schedule
- Readings
- Assignments
- Grading policy
- Forum (TED)
- Content/announcements through TED *

I will assume that you check these daily
- Grades will be posted on Grade Source
Logistics: Textbooks

Required text:


Other references:


• [Lang]: “Digital Systems and Hardware/Firmware Algorithms” by Milos D. Ercegovac and Tomas Lang
In class we will use Clickers!

- Lets you vote on multiple choice questions in real time.
Lecture: Peer Instruction

• I will pose carefully designed questions. You will
  – Solo vote: Think for yourself and select answer
  – Discuss: Analyze problem in teams of three
    • Practice analyzing, talking about challenging concepts
    • Reach consensus
    • If you have questions, raise your hand and I will come over
  – Group vote: Everyone in group votes
  – Class wide discussion:
    • Led by YOU (students) – tell us what you talked about in
      discussion that everyone should know!
Why Peer Instruction?

• You get to make sure you are following the lecture.
• I get feedback as to what you understand.
• It’s less boring!
• Research shows it promotes more learning than standard lecture.
Logistics: Course Components

Grading (grade on style, completeness and correctness)
• iClicker: 3% (12 out of 15 classes)
• Homework: 7% (grade based on a subset of problems. If more than 70% of class fills CAPEs, best 4 out of 5 )
• Midterm 1: 30% (T 4/22)
• Midterm 2: 30% (T 5/13)
• Midterm 3: 30% (Th 6/05)
• Optional take home final exam due 10PM, Th 6/12: 1% bonus
• Grading: Absolute:  A->90% ,  pass (C-)≥ 40% pass
We will consider the curve.
A word on HWs and exams

• HWs:
  – Practice for exams
  – Do them individually for best results

• Exams
  • (Another) Indication of how well you have absorbed the material
  • View exam results as objectively as possible
  • Learn from mistakes and move on ….
Course Problems…Cheating

• What is cheating?
  – Studying together in groups is encouraged
  – Turned-in work must be completely your own.
  – Copying someone else’s solution on a HW or exam is cheating
  – Both “giver” and “receiver” are equally culpable

• Cheating on HW/ exams: in most cases, F in the course.
• Any instance of cheating will be referred to Academic Integrity Office
Motivation

• Microelectronic technologies have revolutionized our world: cell phones, internet, rapid advances in medicine, etc.

• The semiconductor industry has grown from $21 billion in 1985 to $268 billion in 2007.
The Digital Revolution

Integrated Circuit: Many digital operations on the same material

Vacuum tubes

ENIAC

Stores Program Model

WWII

1949

Integrated Circuit

(1.6 x 11.1 mm)

Exponential Growth of Computation

Moore’s Law

1965
Robert Noyce, 1927 - 1990

- Nicknamed “Mayor of Silicon Valley”
- Cofounded Fairchild Semiconductor in 1957
- Cofounded Intel in 1968
- Co-invented the integrated circuit
Gordon Moore

• Cofounded Intel in 1968 with Robert Noyce.

• **Moore’s Law**: the number of transistors on a computer chip doubles every 1.5 years (observed in 1965)
Technology Trends: Moore’s Law

Since 1975, transistor counts have doubled every two years.
Principle of Abstraction

Abstraction: Hiding details when they aren’t important
Scope

• The purpose of this course is that we:
  – Learn the principles of digital design
  – Learn to systematically debug increasingly complex designs
  – Design and build digital systems
  – Learn what’s under the hood of an electronic component
We will cover four major things in this course:

- Combinational Logic (Harris-Chap 2)
- Sequential Networks (Harris-Chap 3)
- Standard Modules (Harris-Chap 5)
- System Design (Harris-Chap 4, 6-8)
Scope: Overall Picture of CS140

Data Path Subsystem

- Memory File
- Pointer
- Select
- Mux
- ALU
- Memory Register
- Conditions

Control Subsystem

- Conditions
- Sequential machine
- Control
- CLK: Synchronizing Clock
Combinational Logic vs Sequential Network

**Combinational Logic:**

\[ y_i = f_i(x_1, \ldots, x_n) \]

**Sequential Networks**

1. Memory
2. Time Steps (Clock)

\[ y_i^t = f_i(x_1^t, \ldots, x_n^t, s_1^t, \ldots, s_m^t) \]

\[ S_i^{t+1} = g_i(x_1^t, \ldots, x_n^t, s_1^t, \ldots, s_m^t) \]
## Scope

<table>
<thead>
<tr>
<th>Subjects</th>
<th>Building Blocks</th>
<th>Theory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinational Logic</td>
<td>AND, OR, NOT, XOR</td>
<td>Boolean Algebra</td>
</tr>
<tr>
<td>Sequential Network</td>
<td>AND, OR, NOT, FF</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>Standard Modules</td>
<td>Operators, Interconnects, Memory</td>
<td>Arithmetics, Universal Logic</td>
</tr>
<tr>
<td>System Design</td>
<td>Data Paths, Control Paths</td>
<td>Methodologies</td>
</tr>
</tbody>
</table>
Part I. Combinational Logic

Next Lecture Reading:
[Harris] Chapter 2, Section 2.1-2.4