VASILEIOS KONTORINIS

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Objective & Interests

An R&D position related to my research interests in computer architecture: analytical modeling of processor performance and power, low-power adaptive microprocessor design, scheduling for multi-core and multi-threaded environments, data center design and cost analysis.

Education

University of California, San Diego, (Sept 2006 - Expected graduation Fall 2012)
Doctor of Philosophy in Computer Science
Advisors: Dean Tullsen, Tajana Simunic Rosing
Thesis: "Adaptive Architectures for Peak Power Management"

University of California, San Diego, (Sept 2006 - Summer 2009)
Master of Science in Computer Engineering (Graduate GPA: 3.92/4.0)

University of Patras, Greece (Feb 2006)
Bachelor of Electrical Engineering (Minor in Computer Science and Microelectronics)
Advisor: Stefanos Kaxiras (GPA: 8.81/10.0)
Summa cum laude, with Honors (Ranked 1st out of 250)

Research Projects

Managing data center peak power with battery enabled power capping

Investigated the use of battery energy for power capping in data centers with distributed UPS. Our approach discharges UPS batteries during high demand hours and recharges them during low demand, on a daily basis. We flatten power profile and allow additional servers within the provisioned power, which better amortizes infrastructure costs. [ISCA 2012]

Contributions:

- Achieved 23% power oversubscription, 6.2% TCO/server reduction at no performance loss.
- First to propose Lithium Iron Phosphate instead of Lead-acid technology for UPS batteries.
- Devised a methodology to optimize battery properties for power capping.
- Designed a controller that orchestrates the charging and discharging of batteries.
- Implemented an event-driven data center simulator (~5K LOC in python/pypy/SimPy).
- Modeled data center Total Cost of Ownership (TCO) to quantify the benefits of power oversubscription (in Excel, released under FreeBSD).

Peak power management at the microprocessor level

Conceptualized a new core design that reduces peak power of the processor through centrally controlled resource adaptation. This design keeps a portion of the core, the least required for performance, constantly power-gated. [MICRO 2009]

Contributions:

- Demonstrated peak power reduction of ~30% at the cost of ~5% performance degradation.
- Introduced a table driven approach to enforce power caps. Each core can be only in a configuration from a hard-coded table.
- Developed a methodology for populating the configuration table.
- Implemented dynamic core reconfiguration in Smtsim simulator (~10K LOC C/C++).

Resource sharing in 3D integrated Cores

Introduced a new alternative to the 3D chip design space: an architecture that supports on demand core resource sharing across 3D-stacked dies. Vertical resource pooling, using through-silicon vias, allows embedded-like cores perform comparably to bigger, high-end designs while thermals remain manageable. [HPCA 2012]

Contributions:

- Showed performance gains of 9-41% and significant energy efficiency boost.
- Designed allocation and arbitration algorithms for shared back-end processor resources.
- Implemented resource pooling across cores in Smtsim simulator (~8K LOC C/C++).

Virtual Machine consolidation for power savings

Motivated the co-locating of latency sensitive with throughput oriented virtual machines to increase power efficiency. Demonstrated a running framework for resource managemet of both service and batch VMs. [VHPC 2012]

Contributions:

- Demonstrated improvements in average work done per joule of 10-30%.
- Introduced qMIPS/Watt metric to measure useful work done while meeting Service Level Agreements.
- Created an infrastructure to automate overnight generation of experiments. The framework could remotely start/stop/move VMs through Xen API, start/stop applications inside the guest VMs, collect statistics through IPMI interface and an external power meter.
- Installed and maintained Olio, a web 2.0 social networking application.

Working Experience

Sun Microsystems, Inc. (currently Oracle), Solaris Kernel Team • Research/SDE Intern
Menlo Park, CA • Summer 2008 • Supervisor: Darrin Johnson

Responsibilities:

- In a team of two modified Open-Solaris scheduler to use performance counter feedback.
- Implemented benchmarks to stress pipeline and memory subsystem.
- Conducted extensive experiments on Niagara T2 and quad-core Xeon processors.

Key Results:

- Developed a scheduler prototype that categorizes applications based on transiency, memory-intensiveness.
- Work was partially incorporated into the commercial Solaris 10 scheduler.
- Work was published in ISLPED 2009.

Conexant Systems, Inc • Embedded Systems Driver Software Development Intern
La Jolla, CA • Summer 2007 • Supervisor: Adrian Kwong

Responsibilities:

- Contributed to the power management design of Conexant's set-top box chipset.
- Learned about low-power software features and ARM architectures.

Key Results:

- Wrote 2-3K lines of code (50% ARM assembly, 50% C) to execute programs directly from ARM1176 cache and turn off memory controller.
- Developed a mini boot loader for code validation and testing.

University of California, San Diego • Teaching Assistant

Responsibilities:

- "Introduction to Computer Architecture"*(CSE141)* course; lectured in discussion hours, graded assignments and projects. (Winter 2009 – instructor Dean Tullsen)
- "Computer Architecture Lab"*(CSE141L)* course; supervised students while implementing in Verilog their own custom-ISA processor. Held office hours, graded final project. (Summer 2009 – instr. Isaac Chu, Fall 2009 – instr. Steven Swanson)

Awards & Activities

- **External Reviewer** for IGCC 2010, TACO 2010, CF 2011, ISCA 2011.
- **Best Student Poster Award**, Multi-scale System Center, 2011.

- **Jacob's Graduate Student Fellowship**, University of California, San Diego, , 2006-2009.
- **Award** for ranking in class top 2%, I.K.Y. (National Scholarship Foundation) (2000- 2005)
- **Scholarship** for excellent GPA (top 1% in University of Patras), T.E.E. (Technical Chamber of Greece).

Publications

1. **V.Kontorinis**, L.Zhang, B.Aksanli, J.Sampson, H.Homayoun, E. Pettis, D.Tullsen, T.Rosing ."Managing Distributed UPS Energy for Effective Power Capping in Data Centers." (**ISCA** 2012)
2. **V.Kontorinis,** J.Sampson, L.Zhang, B.Aksanli, H.Homayoun, T.Rosing, D.Tullsen. "Battery Provisioning and Associated Costs for Data Center Power Capping. (**UCSD Technical Report**, CS2012-0985, 2012)
3. H.Homayoun, M.Rahmatian, **V.Kontorinis**, S.Golshan, D.Tullsen."Hot Peripheral Thermal Management to Mitigate Cache Temperature Variation." (**ISQED** 2012)
4. H.Homayoun,**V.Kontorinis**, A.Shayan, T.Lin, D.Tullsen."Dynamically Heterogeneous Cores Through 3D Resource Pooling." (**HPCA** 2012)
5. G.Dhiman, **V.Kontorinis**, R.Ayoub, L.Zhang,C.Sadler, D.Tullsen, T.Rosing."Themis: energy Efficient Management of Heterogeneous Workloads in Data Centers." (**VHPC Workshop** 2012)
6. G.Dhiman, **V.Kontorinis**, E.Saxe, J.Chew, T.Rosing, D.Tullen, T.Rosing."Dynamic Workload Characterization for Power Efficient Scheduling on CMP systems." (**ISLPED** 2010)
7. **V.Kontorinis**, A.Shayan, R.Kumar, D.Tullen. "Reducing Peak Power with a Table-Driven Adaptive Processor Core." (**MICRO** 2009)

Skills

Programming:	C/C++ (proficient), Python (proficient), R, MATLAB, Perl, Java, Dot, Mysql, Awk, Bash, Hspice, Verilog, Intel/ARM/MIPS assembly (competent)
Operating Systems:	Linux, Unix, and Windows
Source control:	RCS, SVN, Mercurial, Git
Virtualization:	Xen, VirtualBox, VMware

References are available upon request.