μ*DSim*, a Microprocessor Design Time Simulation Infrastructure

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The complexity associated with the design of high performance processors is increasing rapidly. Designers constantly expand the sophistication and scope of the functionality found in their designs. This makes estimating how much time it takes to design and verify these designs increasingly difficult. The design of a modern processor is a resource intensive endeavor, however there has been little work [3] done on measuring, understanding, and estimating the effort it requires.

While there are several analytical and simulation infrastructures developed by the computer architecture community to address the modelling, prediction of traditional metrics such as power/performance/temperature, there has been virtually no work done to predict processor design time. The lack of quantitative approaches to the estimation of the design time overhead means that certain architectural proposals which may have a favorable evaluation based on traditional metrics can have a significant impact on the time required to implement them. Therefore, quantitative approaches used to evaluate the merit of architectural ideas tend to only present a partial picture to the architect, in the sense that complexity and implementation costs are left outside the scope of most evaluations. This omission is significant at a time when design time and costs are becoming clear limiters for the computer architecture community.

The development of quantitative approaches to estimate design costs is still in its infancy. Some existing proposals [3] use analytical models to estimate design effort. By analyzing existing processor designs, [3] is able to isolate a set of metrics that are highly correlated with design effort [1]. In this case, the analytical equation used to model design effort shares similarities with analytical models developed by the software engineering community to predict design effort on software projects. To our knowledge, all these works use an equation or systems of equations.

While analytical models have many advantages, simulation infrastructures can deal with more complex interactions. This distinction is understood by architects that tend to use analytical models for quick estimations but perform detailed simulations to validate their proposals. A group of engineers working together to develop a new design, clearly perform many subtle and complex interactions. Current state of the art works [1, 3, 4] propose to use relatively simple equations to estimate design effort. They can do so at the expense of accuracy and/or difficulty to find the correct tuning parameters.

This paper introduces a simulation infrastructure, μ*DSim* to predict processor design time. The proposed μProcessor Design Simulator (μ*DSim*) has many similarities with industrial process simulation, as well as social simulation games such as Sim City [2]. Instead of a virtual social network as in SimCity, the proposed simulator "models" a processor design team.

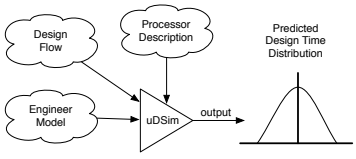

Figure 1: μ*DSim* infrastructure.

μ*DSim* has three major components: engineers, design flow, and processor specification. Furthermore, the interactions needed between designers to partition the work, understand the problem, and implement the processor components, are fully modeled.

μ*DSim* allows the architect to specify the whole processor description or specific processor components by using very high level design description or through metrics like Cyclomatic complexity [5]. The characteristics of the organization teams involved in the implementation of the processor can be described and the simulation infrastructure provides sufficient parametric capacity to do so. Based on the processor description and team organization, μ*DSim* simulates the design process under typical industry project development process. The simulator provides support for typical communication/interaction patterns between engineers, learning skills and some other parameters in the engineers model. Due to the fact that multiple random factors are at play when modeling design processes, μ*DSim* performs several simulations to provide the architect with a feedback consisting of a distribution of the average design time and the associated standard deviation for the given architecture.

μ*DSim* can be used to estimate the overall time to complete a processor and also to estimate the additional time required to implement an architectural modification. We used μ*DSim* on SEED [6], a previously proposed issue logic that delivers performance, power, and area improvements,μ*DSim* reports that the SEED requires 8% additional design time when implemented on an Alpha-like processor. If we assume that processors double performance every 24 months, the SEED design time delay represents a 6% slowdown.

[1] Design effort is different from design time. Design effort is the time required to implement a project if a single person does it. Design time is the time to complete the project by a team.

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