Heterogeneous Stacked-Silicon Interconnects

- Introduce heterogeneous stack silicon FPGAs which is a die with FPGAs and some other IC on a single package combined with a passive silicon interposer
  - The BGA balls are at the lowermost floor that connect the ceramic substrate and then c4 bumps are between the ceramic package and the passive silicon interposer.
  - Microbumps are the connection interface between the interposed and the actual FPGA or “GTZ-IC” chip.
  - The main technology that helps enable this is the “TSV” through silicon Via
- As number of transistors increase, takes longer to get to production
  - 2M logical cells ~ 7 billion transistors
  - Alternative: Combine 4 dice each with ¼ of transistors
  - Scalability is improved
  - “Capacity beyond Moore’s law”
- Traditional MCM/PCB, multiple chips from different companies connected through a PCB.
- Replace the PCB with an interposer, which is a metal “die” connecting the multiple dies sitting side by side, so it’s 2.5D.
- Final step is full 3D stack, chip on chip. Haven’t gotten here yet need the tech to improve for this to happen.
- You can integrate both Analog and digital IP’s together and yield optimize both for die for performance
  - They show a serial transmitter simulated and actual and show that the FPGA performance for this is actually as good as the actual serial transmitter.
  - Originally the problem is that there is a lot of noise when trying to hook up the FPGA with other analog signals, but with the interposer it lets the communication channel be a lot cleaner and the signal is seen to be close to an actual serial transmitter
- They describe two different kinds of interconnects that allow for clean communication and let the heterogeneous chips to actually work.
  - The type 1: is between the IC and package which is two different microbumps in a chip connected through the TSV through the interposer to the c4 bumps down to the bga balls
  - The type 2: is between different chips and works as the microbumps pass through the passive silicon interposer
    - each microbump has a micro bump pad and when going from one IC to another goes through clocks or signals and shields in the interposer layer