7 Series DSP48E1 Slice

**DSP48E1 Features**

- They implemented a dedicated DSP in a slice because FPGAs are efficient for DSP apps due to their parallel nature. Use Binary multipliers/accumulators and are implemented in slices.
- The difference from previous version is that this one is wider and has SIMD mode, and an ALU, pattern detector and shifter.
- The DSP is automatically used for arithmetical functions but have many applications in which the DSP excels at
  - Pipeline for performance and lower block
  - Use CLB/CLB DR to store filter coefficients
  - Cascade using the DSP instead of fabric to keep usage only on ONE COLUMN for best performance and power
- The DSPs cannot be cascaded across the interposer SLR

**DSP48E1 Description and Specifics**

- The DSP support multiply, accumulate, among other mathematical bitwise operations
- The actual slice has a multiplier and accumulator and needs three pipeline registers for multiply and multiply-accumulate.
- The DSP supports sequential and cascaded operations for applications: FFT, floating point, computation, counters, etc.
- A DSP tile is created by two DSP slices with a dedicated interconnected and are stacked vertically in a DSP column.
  - The height of this is the same as 5 CLBs and matches the height of one block RAM
  - Each DSM slices is as long as a 16K block RAM and there are up to 20 DSP columns
- The ports on the slice support many DSP and arithmetic operations and algorithms

**DSP48E1 Design Considerations**

- For best performance the DSP should be fully pipelined
  - For multiplier designs you need to use a three stage pipeline
  - for non multiplier designs a two stage pipeline is used
- For best power usage you can turn off the multiply and other parts when just doing add/logic unit operations.
  - In addition using cascade instead of fabric routing also reduces power
  - A multiplier with M register turned on uses more power than M off
- Usually fabric adders are the performance bottleneck. Instead they end up using a CLB that utilizes the LUTS and carry chain for a ternary adder
- Adder cascade uses the cascade path in the DSP to do the post addition process of the adder.