**Xilinx 7 Series FPGA Overview**

- **SSI Technology**
  - Enables multiple super logic regions (SLR) to be combined on an interposer.
    - (This is their 2.5D technology)
      - Logic intensive SLR and a DSP SLR
- **CLB**
  - The control logic blocks have look up tables, each LUT can be registered in a flip flop. A combination of four LUTS with eight flip flops and muxes/ALU are called a slice. One of the CLBs have two of these kinds of slices in them. (They have a DSP Slice)
- **Clocks**
  - Three kinds of dividers, DMO
    - D: Pre-divided, reduces input frequency
    - M: Feedback divided programming by configuration is a multiplier
    - O:
- **Block RAM**, each has two independent ports sharing nothing but stored data
  - Can be used to have programming data width, each BR can be divided into independent 19kb block RAMS for any ‘aspect ratio’
  - Has a built in FIFO controller for single or dual block operation increments
- **I/O Logic**: All I/O can be configured as combinatorial or registered and works with DDR rates
  - Varies with package and is configurable for many IO standards
  - The high range and IO pins are organized in banks with 50 pins per bank, each bank has
  - Each pin has a 8-bit IOSERDES for serial to parallel conversions
- **Low-Power Gigabit Transceivers**
  - Capable of up to 28Gb/s and low power mode for chip to chip interfaces
  - Transmitter: parallel to serial converter
  - Receiver: Serial to parallel converter
  - Out of band signaling is provided by the transceiver for sending low speed signals from transmitter to receiver
- **PCI-E Designs**: There includes at least one PCI-E integrated block for that can configured as an Engine or root port for 2.1 or PCI 3.0. This is useful for FPGA to FPGA communication via PCI and attached ethernet controller or fibre channel HBA’s to the FPGA.
  - It is highly configurable and can go up to 8 lanes up to 8Gb/s data rates
- **XADC**: Analog to digital converter, is provided. Two ADC can be configured to simultaneously sample two external input analog channels.