

ON THRESHOLD CIRCUITS FOR PARITY

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ABSTRACT

Motivated by the problem of understanding the limitations of neural networks for representing Boolean functions, we consider size–depth trade–offs for threshold circuits that compute the parity function. It is well-known that the parity function on n variables can be computed by a depth–2 threshold circuit with a quadratic number of edges. It is not hard to construct such a circuit with a linear number of edges in depth $O(\log \log n)$ and in fact there is a construction that provides a transition between these extremes.

Our starting point was an attempt to show that the trade–off exhibited by this construction is the best possible. The result we present in this paper is an almost optimal lower bound $\Omega(n^2/\log^2 n)$ on the number of edges for computing parity function with depth–2 threshold circuits whose weights are bounded by a polynomial in n . (We get a much sharper lower bound of $\Omega(n^2)$ in the case when all the weights of the first level gates are nonnegative or of the form ± 1 .) While this result falls short of our goal, its proof involves an interesting application of *rational approximation theory* to complexity theory. The technique holds promise towards a complete answer to this trade-off question and also seems to be a natural and a potentially useful approach to the analysis of threshold circuits in general. Such an approach might also be relevant to the solution of the question whether TC^0 (the class of functions computable by bounded depth and polynomial size threshold circuits) is equal to NC^1 (the class of functions computable by fan-in 2 log–depth Boolean circuits).

The question of lower bounds on the size of depth–2 circuits for parity is closely related to the following *open* problem: What is the minimal number of hyperplanes required to intersect all the edges of the unit hypercube? We show that a lower bound of $f(n)$ on the number of hyperplanes would imply an $\Omega(nf(n))$ lower bound on the edge complexity for computing parity with depth–2 circuits.

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