ADVANCE PROGRAM
HOT CHIPS 22

A Symposium on High-Performance Chips
August 22-24, 2010, Memorial Auditorium,
Stanford University, Palo Alto, California

HOT CHIPS brings together designers and architects of high-performance chips, software, and systems. Presentations focus on up-to-the-minute real developments. This symposium is the primary forum for engineers and researchers to highlight their leading-edge designs. Three full days of tutorials and technical sessions will keep you on top of the industry.

Sunday August 22

Morning Tutorial — Non-Volatile Memory

• Forging a Future in Memory	Ed Dollar	**Micron**
• Status and Prospect for MRAM Technology	Saied Tehrani	**Everspin**
• Metal Oxide RRAM as a Future Non-Volatile Memory	Paul Kirsch	**Sematech**
• Solid-State Disks in Enterprise Systems	TBD	
• Storage Class Memory	Richard Freitas	**IBM**

Afternoon Tutorial — Optical Interconnects

• Overview: VCSELs to Silicon Nanophotonics	Ashok Krishnamoorthy	**Oracle**
• Silicon photonics in the data center	Al Davis	**U. of Utah, HP Labs**
• Silicon photonics and memories	Vladimir Stojanovic	**MIT**
• Hybrid on-chip data networks	Gil Hendry	**Columbia**
• Multi-chip photonic network	Frankie Liu	**Sun Labs, Oracle**

Monday August 23

High Performance Computing

- Fermi GF100: A GPU For Compute, Tessellation, and Computational Graphics — **NVIDIA**
- End of Scaling of Traditional Microprocessors — **Schlumberger, Stanford**
- Adaptive Energy Management Features of POWER7 — **IBM**

Keynote 1 **Hartmut Neven** — **Google**
Searches Originating Inside and Outside of Your Head

SoCs

- The New Xbox 360 SoC — **Microsoft**
- Extensions to the ARM v7-A Architecture — **ARM**
- Solving 4G Challenges with Multi-Core Baseband SoCs — **Mindspeed**
- GreenDroid: A Mobile Application Processor for a Future of Dark Silicon — **UCSD, MIT**

Networking & the Data Center

- A Wire-Speed Processor: 16 POWER(r) Cores with 64 Threads per Core — **IBM**
- Smart Memory for High-Performance in Network Packet Forwarding — **Huawei**
- iMB™:Enabling Low-Power Cloud Computing and Server Virtualization — **Inphi**

Panel: Asia: Partner or Competitor?

Tuesday August 24

FPGAs

- 28nm Generation Programmable Families — **Xilinx**
- Stratix V with 28Gbps Transceivers in 28nm — **Altera**
- 3D FPGA for Improved Density, Power and Performance — **Tier Logic**

Interconnects

- ICC:An Interconnect Controller for the Tofu Architecture — **Fujitsu**
- The Hub Module in 45nm CMOS SOI : A Terabyte Interconnect Switch — **IBM**
- Silicon Photonics: Optical Connectivity at 25 Gbps and Beyond — **Luxtera**
- Spidergon STNoC: Network-on-Chip Gives Added System Value — **ST Microelectronics**

Keynote2 **Burkhard Huhnke** — **VW Palo Alto Lab**
Electronics in Cars

Servers

- Westmere-EX: A 20-Thread Server CPU — **Intel**
- Architectural Innovations in Westmere-EP — **Intel**
- GS464V: A High-Performance Low-Power XPU with a 512-Bit Vector Extension — **Chinese Academy of Sciences**

New Processor Architectures

- The Next-generation System z Micro-Processor — **IBM**
- AMD's "Bulldozer" Core – Multi-Threaded Compute Performance for Maximum Efficiency and Throughput — **AMD**
- AMD's "Bobcat" x86 Core – Small, Efficient and Strong — **AMD**

Please visit us on the web: **http://www.hotchips.org**
or drop us a line via Email: **info2010@hotchips.org**

IEEE computer society

This is a preliminary program; changes may occur. For the most up-to-the-minute details on presentations and schedules, and for registration information, please visit our web site where you can also check out HOT Interconnects (another HOT Symposium being held following HOT CHIPS)

SSCS IEEE

A Symposium of the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society and the Solid State Circuits Society