New Insights into the Design for End-of-life Variability of NBTI in Scaled High-$\kappa$/Metal-gate Technology for the nano-Reliability Era

Pengpeng Ren1, Runsheng Wang1,2, Zhigang Ji3,4, Peng Hao1, Xiaobo Jiang1, Shaofeng Guo1, Mulong Luo1, Meng Duan1, Jian F. Zhang2,3, Jianping Wang1, Jinhua Liu1, Weihai Bu1, Jingang Wu1, Waisong Wong2, ShaoFeng Yu3,5, Haoming Wu5, Shiuh-Wuu Lee3,5, Nuo Xu4, Ru Huang1,5,*

1Institute of Microelectronics, Peking University, Beijing 100871, China (Emails: ruhuang@pku.edu.cn, r.wang@pku.edu.cn)
2School of Engineering, Liverpool John Moores University, Liverpool L3 3AF, UK (Emails: z.ji@ljmu.ac.uk, j.f.zhang@ljmu.ac.uk)
3Semiconductor Manufacturing International Corporation (SMIC), Shanghai 201203 and Beijing 100176, China
4Department of EECS, University of California, Berkeley, CA 94720, USA
5Innovation Center for MicroNanoelectronics and Integrated System, Beijing 100871, China

Abstract

In this paper, a new methodology is proposed for the assessment of end-of-life variability of NBTI is proposed for the first time. By introducing the concept of characteristic failure probability, the uncertainty in the predicted 10-year $VDD$ is addressed. Based on this, variability resulted from NBTI degradation at end of life under specific $VDD$ is extensively studied with a novel characterization technique. With the further circuit level analysis based on this new methodology, the timing margin can be relaxed. The new methodology has also been extended to FinFETs in this work. The wide applicability of this methodology is helpful to future reliability/variability-aware circuit design in nano-CMOS technology.

Introduction

As CMOS devices downscaling into nanoscale region, dynamic variability induced by NBTI effects has been paid growing attention [1-10]. With device aging, the induced variations will directly degrade the circuit stability [2-5], which is especially significant at end of life in more aggressive technology nodes (Fig. 1). Therefore, assessment of the end-of-life variability emerges as a big necessity for practical circuit design in the nano-reliability era, including both the impacts of device-to-device variation (DDV) [1, 3, 7-9] and the cycle-to-cycle variation (CCV) recently found in our work [9-10]. However, it faces great challenges: The conventional assessment methodology is not suitable for characterizing NBTI variability and the resulted variability in nano-devices, due to the stochastic nature of trapping/detrapping within the gate oxide [6-10]. New methodology is thus intensively required.

In this paper, a new methodology is proposed to address the challenges in characterizing the end-of-life variability for nanoscale devices, with demonstrations on high-$\kappa$/metal-gate (HKMG) and FinFET technology for the first time. By introducing the novel characterization technique, variability induced by the NBTI degradation at end of life is experimentally studied. The impacts on circuit and yield analysis are also investigated.

New Assessment Methodology for End-of-life Variability

To assess the end-of-life variability, the 10-year $VDD$ should be predicted at first. However, nano-devices brought big challenges into 10-year $VDD$ prediction with conventional constant voltage stress (CVS) procedure [11] in two aspects: (1) Requirements of multiple identical devices in CVS method cannot be met by the severe DDV effect. (2) Time-dependent variability during degradation within a single device (CCV effect) makes the conventional power factor extraction unreliable (Fig. 2). In addition, the method using large devices to predict 10-year $VDD$ also fails, since the degradation of large devices is not consistent with the average degradation of nano-devices (Fig. 3). A new assessment methodology with novel characterization technique is thus required. The underlying physics and models should be also explored, with extension to circuit level analysis (Fig.4).

As shown in Fig. 5, the NBTI degradation in nano-devices manifests large fluctuations. To evaluate the extent of device degradation at end of life for specific $VDD$, the concept of failure probability is introduced in the new methodology, which includes not only the impacts of DDV, but also the transient failure caused by CCV effect. Due to the large variations of the degradation, the conventional definition of 10-year $VDD$ needs to be improved. Rather than a single value, the 10-year $VDD$ becomes probabilistic in nano-devices, and each one is with a characteristic value of failure probability. The 10-year $VDD$ will be determined by the target failure probability in practice. In other words, the end-of-life variability becomes a 2-D problem at specific $VDD$ (Fig. 6): one dimension is the DDV of the mean degradation; the other is the DDV of the fluctuations in the degradation under accelerated stress to normal $VDD$ for end-of-life characterization, novel characterization technique is required, which will be shown next. Devices measured in this work are scaled HKMG planar pFETs and SOI FinFETs.

Novel Fast Voltage Step Stress (FVSS) Technique

A new characterization technique named FVSS is proposed to address the challenges in 10-year $VDD$ prediction for nanoscale devices. By introducing the concept of stepped stressing [12], the 10-year $VDD$ can be predicted on a single device, rather than multiple devices with the impact of DDV. $V_{th}$ sensing method is based on the modified ultra-fast technique [13] to fully capture the CCV effect during degradation. As shown in Fig. 7, the device is continuously stressed by stepped stress $V_{Gstr}$ for the same $\Delta t$ until reaching pre-specified step $N$. The stress bias is interrupted quickly and periodically to monitor the $V_{th}$ shift ($\Delta V_{th}$) within 5s under the same $V_{Gmea}$ ($< V_{Gstr}$). With ultra-fast measurement, $\Delta V_{th}$ can be obtained with higher sampling rate, which enables the extraction of $n$ in the first step of FVSS technique. Due to the gradual increase of $V_{Gstr}$, the degradation is
accelerated (Fig. 8). With Eq. 2, the stress time under high $V_{Gat}$ can be equivalently transformed to effective stress time under the first $V_{Gat}$ ($=V_f$) with the optimal parameters $m$ and $A$ to restore the power law statistics under $V_f$. Thus the 10-year $VDD$ can be predicted on a single device with the extracted parameters. In addition, the effective stress time can be transformed under any $V_C$ bias (e.g., $VDD$) with Eq. 3. The FVSS method is firstly verified with large devices. Good agreement is achieved between the FVSS and conventional CVS methods (Fig. 9). Thus it can be applied to nano-devices (Fig. 10&11). As expected, the $\Delta V_{th}$ manifests large fluctuations against stress time due to CCV effect.

Experimental Results and Discussions

a) Statistics of failure probability: As shown in Fig. 12, the failure probability at specific $VDD$ after transformation can be extracted as the probability that $\Delta V_{th}$ larger than the failure criterion (50mV as an example here) around 10-year lifetime. The extracted failure probability (Fig. 13) presents a large dispersion with varying $VDD$ for nano-device compared with large device, due to CCV effect. With DDV effect further taken into account (Fig. 14), the failure probabilities of different devices have a wider distribution. It can be observed in Fig. 14(c) that DDV is much larger than CCV, mostly due to the fact that the measured devices (30x300 nm$^2$) are not sufficiently small. Thus, for a given $VDD$, the effective occupation probability will be 1 or 0 for most of the devices. As a direct result, the distribution of the failure probability among different devices should be U-shape like, which is consistent with the experimental results in Fig. 15. This interesting behavior will be discussed later in more details with correlation to trap energy distribution.

b) HK process, FinFET and AC NBTI: The mean failure probability is extracted and compared between two HK processes (Fig. 15). HK process #1 presents less degradation and variation due to process optimization. The $VDD$ corresponding to 100% and 0% failure are further extracted and compared in Fig. 16. With the scaling of the gate area, the dispersion of failure probability becomes larger, indicating the more severe impacts of CCV and DDV. Fig. 17 shows the results of FVSS technique applied to FinFETs (Fig. 17), confirming its applicability beyond planar technology. The methodology can also be extended to AC NBTI characterization (Fig. 18). The impact of CCV is also non-negligible under practical AC circuit operation conditions.

c) Degradation and variation at end of life: Once the degradation is transformed under specific $VDD$, the average and deviation values of $\mu(\Delta V_{th})$ and $\sigma(\Delta V_{th})$ among different devices at end of life can be extracted around 10-year lifetime in terms of $\mu(\mu)$, $\sigma(\mu)$, $\mu(\sigma)$ and $\sigma(\sigma)$ respectively, as shown in Fig. 19. Large variations can be observed at end of life, which will directly degrade the parametric yield. With the increase of $VDD$, more traps are generated, contributing to the increase of dynamic variations.

d) Distributions of 10-year $VDD$: From another perspective of statistics, the dispersion of failure probability can be evaluated alternatively by the distribution of 10-year $VDD$ among different devices with the same mean failure probability. The distribution of 10-year $VDD$ well fits Weibull distribution [Fig. 20(a)]. The shape factor of the Weibull distribution keeps the same with the varying failure probability, and decreases with the shrinking gate area [Fig. 20(b)].

Physical Model of Failure Probability

The U-shape like distribution of failure probability is fundamentally correlated with the energy distribution of oxide traps. Fig. 21 shows the trap charge density $N_{ct}$ and energy density $D_{ot}$ extracted in large device with the method in [14]. Since the occupation probability is directly determined by the differences between Fermi level and trap energy level, the distribution of the occupation probability is correlated with the energy distribution of oxide traps (Fig. 22). With the proposed physical model (Eq. 4), the theoretical distribution of failure probability is well consistent with the experiment results. The impact of different energy distribution of oxide traps on failure probability is simulated (Fig. 23). Therefore, the new methodology could also be applied to new materials (e.g. Ge, III-V) which have different trap energy distributions from Si.

Impacts on Circuits and Yield Analysis

Based on the above results, the new methodology is extended to circuit and yield analysis. Considering the severe impacts of DDV and CCV at end of life, the frequency shift of ring oscillator (RO) presents wide distribution with the varying $VDD$ (Fig. 24). The individual RO circuit fails stochastically among the operation cycles due to CCV effect (Fig. 25). In other words, it does not fail in some operation cycles within the ‘dying’ part (Fig. 26), contradicted to the view that the ‘dying’ part is regarded as totally failed in conventional assessment methodology. Therefore, the additional timing margin can be relaxed with the new methodology. On the other hand, the impact on end-of-life parametric yield is also evaluated. With specific failure criterions, the 10-year $VDD$ of RO is determined by the target yield (Fig. 27).

Summary

We have proposed a new methodology for assessing end-of-life variability of NBTI in this paper. The uncertainty in the predicted 10-year $VDD$ is addressed by introducing the concept of characteristic failure probability. At specific $VDD$, the induced variations from NBTI degradation at end of life are extensively studied for the first time with the proposed novel technique. With the further analysis on circuit level, timing margin can be relaxed with the new methodology. It is thus helpful to the variability-aware circuit design in the nano-reliability era.

Acknowledgement

This work was partly supported by the 973 Projects (2011CB00601), NSFC (61106085), National S&T Major Project (2009ZX02035-001).

References

10-year lifetime, the corresponding failure probability is extracted as the probability
of degradation transformed to (a) VDD = 1.2V, (c) VDD = 1.15V, (e) VDD = 1.1V, and (g) VDD = 1.05V. Around
10-year lifetime, the Δ Vth follows the normal distribution. The corresponding failure probability is extracted as the probability that Δ Vth is larger than the failure criterion (50 mV as an example here). The results are shown in (b), (d), (f) and (h) respectively.

The extracted failure probability for a single device with varying VDD, compared with that of a large device. The 10-year VDD is no more a single value, but becomes probabilistic and each with one characteristic value of failure probability.

The degradation transformed to (a) VDD = 1.2V, (c) VDD = 1.15V, (e) VDD = 1.1V, (g) VDD = 1.05V. Around
10-year lifetime, the Δ Vth follows the normal distribution. The corresponding failure probability is extracted as the probability that Δ Vth is larger than the failure criterion (50 mV as an example here). The results are shown in (b), (d), (f) and (h) respectively.
Fig. 15 The extracted mean failure probabilities compared between (a) HK process #1 and (b) HK process #2 with different gate areas. The distributions of the failure probabilities of different devices turn to be U-shape like and are shown in (c), (d) and (e), respectively.

Fig. 16 (a) The 10-year VDD corresponding to 100% failure, 0% failure and (b) their difference $\Delta V = VDD(P=100\%) - VDD(P=0\%)$ with different gate areas. Large dispersion ($\Delta V = 0.5V$) can be observed.

Fig. 17 (a) FVSS method applied to FinFETs. (b) The extracted failure probabilities compared among devices with different gate lengths.

Fig. 18 (a) FVSS method applied to AC NBTI. (b) The extracted failure probabilities compared among devices with different gate widths.

Fig. 19 (a) $\mu$: the average value of the mean degradation, (b) $\sigma$: the deviation value of the mean degradation, (c) $\mu$: the average value of the variation, and (d) $\sigma$: the deviation values of the variation in individual devices at end of life for two HK processes.

Fig. 20 (a) The distributions of 10-year $VDD$ of different devices with the same failure probability, fitted by Weibull distribution with the shape factor in (b).

Fig. 21 The extracted (a) trap charge density $N_c$ and (b) energy density $D_W$ with $E - E_V$ for two HK processes.

Fig. 22 (a) Distributions of the occupation probability of oxide traps. (b) Comparison of the distribution of failure probability between modeling and experiment.

Fig. 23 Simulated energy distributions of oxide traps in (a), (c) and (e), corresponding to the modeled distributions of failure probability in (b), (d) and (f), respectively.

Fig. 24 (a) The 5-stage RO simulated in this work. (b) The distributions of frequency shift ($\Delta f$) in the total operation cycles of 300 ROs with varying $VDD$ under the impacts of dynamic variations.

Fig. 25 The distributions of frequency shift ($\Delta f$) among 500 operation cycles for individual ROs under different $VDD$. 12 ROs are shown examples for each $VDD$.

Eq. 1 Total dynamic variation (DDV + CCV)

$$\mu[V_{th}]=\mu[V_{th}]\Delta_{th}$$

$$\sigma(V_{th})^2 = \sigma(V_{th})^2 \Delta_{th} + \frac{N^2 + 2N + \mu^2}{N}$$

Saturation case: $\sigma^2(\Delta_{th}) = 2N\mu^2$

Worst case: $\sigma^2(\Delta th) = \frac{2\sqrt{N+2}}{N} \mu^2$

Eq. 2 Effective stress time transformation in FVSS

$$\Delta f_{th} (s=1) = A_{th} f^{\alpha} \Delta t$$

$$\Delta f_{th} (s=2) = A_{th} f^{\alpha} \Delta t^2$$

$\Delta t = \Delta t^2$ for $s=2$

Eq. 3 Effective stress time transformation between $\Delta t^2$ and $VDD$

$$\Delta t^2 = \frac{\Delta f_{th}}{A_{th} f^{\alpha}} \frac{1}{VDD^{\alpha}}$$

Eq. 4 Physical model of failure probability

1. Single trap induced $\Delta f_{th}$

$$P(\Delta f_{th} = f_{th}) = \frac{p_{th}}{p_{th}}$$

where $\lambda_{th}$ is the exponential distributed amplitude of single trap $p(E_v=\frac{1}{e^{\left(-\mu E_{VDD} + \nu E_{VDD} \right)}})$

2. Multi traps induced device failure probability

$$P(\Delta f_{th} = \sum_{k=1}^{N} \Delta t_{\lambda k} \Delta_{th}) = \sum_{k=1}^{N} \frac{1}{N!} \sum_{\lambda_k} \lambda_k^{N-1} \exp(-\lambda_k) \frac{\lambda_k^{N-1}}{N!}$$

where $\lambda_k = \Delta t_{\lambda k}$

$$P(\Delta f_{th} = f_{th}) = \frac{p_{th}}{p_{th}}$$

$N$ is the average trap number per device.