

Moein Khazraee

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- Education**
- PhD in Computer Engineering, UC San Diego 2013 - Current
Adviser: Aaron Schulman
Specialization: Computer Systems, Data-center Networking
- Masters in Computer Science, UC San Diego, GPA: 3.97/4.0 2013 - 2016
Adviser: Michael Taylor
Specialization: Computer Architecture
- B.S. in Electrical Engineering, Sharif University of Technology 2008-2013
Majoring in Digital Systems, GPA: 18.39/20.00 (3.84/4.0)
- Publications**
- M. Khazraee, L. V Gutierrez, I. Magaki, M. B. Taylor, "Specializing a planet's computation: ASIC Clouds" *IEEE Micro top picks*, 2017.
 - M. Khazraee, L. Zhang, L. V Gutierrez, M. B. Taylor, "Moonwalk: NRE optimization in ASIC Clouds, or, accelerators will use old silicon" *ASPLOS*, 2017.
 - I. Magaki, M. Khazraee, L. V Gutierrez, M. B. Taylor, "ASIC clouds: specializing the datacenter." *ISCA*, 2016.
 - M. Khazraee, A. R. Zamani, M. Hallajian, S. P. Ehsani, H. A. Moghaddam, A. Parsafar, M. Shabany. "A novel hardware implementation for joint heart rate, respiration rate, and gait analysis applied to Body Area Network." *ISCAS*, IEEE, 2013.
 - M. R. Homaeinezhad, M. Khazraee, M. Khazraee. "An Open-Source High Speed C++/MEX Framework for the Detection and Delineation of Long Duration Ambulatory Holter ECG Events: HSEDF." *International Journal of Information Engineering*, 2.1 (2012): 12-30.
- Research**
- DSPs in Data-center** Jul. 2017 - Present
- Using DSPs to implement an affordable and c-based programmable Network Interface Card. This solution is power efficient with low latency based on integrated 10Gbps interface.
 - This platform can also be used as a middle-box or DMA to memory over PCIe.
 - In horizon: making a development environment for DSP based networking in data-centers.
- ASIC Clouds** Sep. 2015 - Sep. 2017
- Developed a prototypical ASIC Cloud architecture, which are data-centers full of ASICs, emerging in near future.
 - Developed an infrastructure to design the TCO-optimal data-center for these clouds.
 - Showed that technology node selection is a major tool for managing ASIC Cloud NRE, which is the main challenge for ASIC Clouds. This allows the designer to trade off an accelerators excess energy efficiency and cost performance for lower total cost.
- Bioengineering systems** 2011 - 2013
- Biomedical signal processing and digital circuit implementation for wireless medical care system based on Body Area Networks (BAN). Specifically establishing sensor networks through Bluetooth, utilizing MEMS and pressure sensors for gait detection, and ECG and body posture analysis.
 - ECG signal processing for the detection of long duration ambulatory holter ECG events, using C++ (MEX in MATLAB) for high speed

Work Experience	<p>Research Assistant UC San Diego Sep. 2013 - Present</p> <ul style="list-style-type: none"> Evaluating performance and power trade-offs for different architectures such as ASICs, FPGAs, DSPs, ASIPs, and server Processors. <p>Software Engineer Intern Google Apr. 2017 - Jul. 2017 Collaborated with a team of engineers to develop a methodology for TCO analysis for a part of Google's infrastructure (confidential):</p> <ul style="list-style-type: none"> Learned about how TCO is evaluated in large scale datacenters Used different profiling tools such as perf, valgrind to improve C++ program performance.
Activities	<p>President of 'Cultural Iranian Student Association' (CISTA) UC San Diego 2016</p> <p>Head and Executive Director of Promotion Committee Sharif University of Technology</p> <ul style="list-style-type: none"> Sharif Cup 2012, the 1st Sharif open robotics competition Sep.26-28, 2012 Smart Grid Conference Oct. 19-21, 2010
Academic Experience	<p>Teaching Assistant UC San Diego Fall 2014</p> <ul style="list-style-type: none"> Teaching Assistant for Principals of Computer Architecture graduate course <p>Teaching Assistant Sharif University of Technology 2011-2013</p> <ul style="list-style-type: none"> Instructor for "Verilog" part of "Logic Circuits and Digital Systems" course (three semesters), recreated a new syllabus Member of design group for "Embedded Systems' Laboratory" Revised lab experiments and instructions for "Structure of Computer and Microprocessors Laboratory" <p>Teacher Allame Helli 5 (NODET) Junior High School 2012-2013</p> <ul style="list-style-type: none"> Computer Algorithms • Web Programming <p>Major overhaul of the Microprocessor Lab., Sharif University of Technology 2012</p> <ul style="list-style-type: none"> I took responsibility for instructional and interior improvement in Microprocessor's Laboratory, in which courses such as EE25723 (Microprocessor's System Laboratory) and EE25776 (FPGA and ASIC Systems' Design) were taught. <p>Conference Reviewer, IEEE BIOCAS 2012 - Present</p>
Technical Skills	SystemVerilog, C/C++, Python, Java, VCS, Design Compiler, Quartus, ModelSim, Keil uVision, Matlab, Vivado HLS, JavaScript
Awards & Talks	<ul style="list-style-type: none"> Fellowship for Technology Management and Entrepreneurism certificate program in Institute of Global Entrepreneurship, UCSD 2017-2018 Poster Presentation at the Center for Future Architecture Research Dec. 2016 Qualcomm FMA Fellowship 2015-2016 Fellowship for Ph.D. from University of California San Diego 2013-2014 Privileged project winner for "Biomedical signal processing and digital circuit implementation for wireless medical care system based on Body Area Networks (BAN)", Electrical Engineering top projects competition Jun. 2012 Scholarship for Minor in English, Sharif University of Technology 2010-2013 Ranked amongst top 0.1% in the Nationwide University Entrance Exam 2008
Graduate Coursework	Parallel Computer Architecture, Advanced Micro-architecture, Validation and Prototyping of Embedded Systems, Operating Systems, Advanced Compiler Design, Data Mining and Analytics, Principle of Database Systems, Data Communication Networks, Computer Interface Circuits