Conservation Cores: Energy-Saving Coprocessors for Nasty Real-World Code

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This Talk

The Dark Silicon Problem

How to use Dark Silicon to improve energy efficiency
(Conservation Cores)

The GreenDroid Mobile Application Processor
Where does dark silicon come from? And how dark is it going to be?

The Utilization Wall:

With each successive process generation, the percentage of a chip that can actively switch drops exponentially due to power constraints.

[Venkatesh, Chakraborty]
We've Hit The Utilization Wall

Utilization Wall: With each successive process generation, the percentage of a chip that can actively switch drops exponentially due to power constraints.

- **Scaling theory**
  - Transistor and power budgets are no longer balanced
  - Exponentially increasing problem!

- **Experimental results**
  - Replicated a small datapath
  - More "dark silicon" than active

- **Observations in the wild**
  - Flat frequency curve
  - "Turbo Mode"
  - Increasing cache/processor ratio
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**Classical scaling**

<table>
<thead>
<tr>
<th></th>
<th>classical scaling</th>
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<tbody>
<tr>
<td>Device count</td>
<td>( S^2 )</td>
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<tr>
<td>Device frequency</td>
<td>( S )</td>
</tr>
<tr>
<td>Device cap (power)</td>
<td>( 1/S )</td>
</tr>
<tr>
<td>Device ( V_{dd} ) (power)</td>
<td>( 1/S^2 )</td>
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<td><strong>Utilization?</strong></td>
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**Leakage-limited scaling**

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<tr>
<td>Device count</td>
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<td>Device frequency</td>
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<td>Device cap (power)</td>
<td>$1/S$</td>
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<tr>
<td>Device $V_{dd}$ (power)</td>
<td>$1/S^2$</td>
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<td>Utilization ?</td>
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![Expected utilization for fixed area and power budget](chart.png)
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![Utilization Graph]

- **Utilization @ 40 mm², 3 W**
  - 90 nm TSMC: 5.0%
  - 45 nm TSMC: 1.8%
  - 32 nm ITRS: 0.9%
  - 2.8x reduction
  - 2x reduction
  - 0.9% utilization
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The utilization wall will change the way everyone builds processors.
Utilization Wall: Dark Silicon Leads to Dark Implications for Multicore

Spectrum of tradeoffs between # of cores and frequency

Example: 65 nm → 32 nm (S = 2)

Industry’s Choice

4 cores @ 1.8 GHz

2x4 cores @ 1.8 GHz
(8 cores dark, 8 dim)

(Industry’s Choice)

4 cores @ 2x1.8 GHz
(12 cores dark)

65 nm

32 nm
This Talk

The Dark Silicon Problem

How to use Dark Silicon to improve energy efficiency (Conservation Cores)

The GreenDroid Mobile Application Processor
What do we do with Dark Silicon?

- **Idea:** Leverage dark silicon to “fight” the utilization wall

- **Insights:**
  - Power is now more expensive than area
  - Specialized logic has been shown as an effective way to improve energy efficiency (10-1000x)

- **Our Approach:**
  - Fill dark silicon with specialized energy-saving coprocessors that save energy on common apps
  - Only turn on the cores as you need them
  - Power savings can be applied to other programs, increasing throughput

*Energy saving coprocessors provide an architectural way to trade area for an effective increase in power budget!*
Example: Today's smartphone

- Consumers demand rich functionality (desktop → mobile)

- Utilization Wall still applies
  - Active Power budget is set by
    (battery capacity) / (# hrs active use between recharges)
    rather than thermal design point.

- Still need to reduce computation energy
Using accelerators to reduce energy

- Smartphones already combine a general-purpose processor with specialized coprocessors known as accelerators.

- Audio, Video, Images, Graphics

- Accelerators usually speed up computation and reduce energy.

- Accelerators exist for “easy-to-parallelize”, or regular, code:
  - Well-structured
  - Moderate or High Parallelism
  - Predictable memory accesses and branch directions
  - Relatively small # of lines of code
  - Often requires human guidance to create (#pragmas or worse)
But what about irregular code?

- Many applications use irregular, difficult-to-parallelize code, for which no accelerators exist.

- Amdahl's Law: Overall energy efficiency depends on the fraction of the total code that is optimized!

- To gain large energy savings through specialization:
  - We need energy-saving coprocessors that target irregular code, and
  - We need many, many such coprocessors to get high coverage
    - need to solve both design effort and architectural scalability problems.

100x better

only 1.25x overall
Conservation Cores (C-cores)

"Conservation Cores: Reducing the Energy of Mature Computations," Venkatesh et al., ASPLOS '10

- Specialized coprocessors for reducing energy in irregular code
  - Hot code implemented by c-cores, cold code runs on host CPU;
  - Shared D-cache
  - Patching support for hardware

- Fully-automated toolchain
  - No “deep” analysis or transformations required
  - C-cores automatically generated from hot program regions
  - Drop-in replacements for code
  - Design-time scalable

- Energy-efficient
  - Up to 18x for targeted hot code
The C-core Life Cycle

(a) Stable applications

(b) Patchable c-core specifications

(c) Conservation cores

(d) Many-core processor with c-cores

(e) Patching-Aware Compiler

Versions released over time
Constructing a C-core

- C-cores start with source code
  - Irregular or regular programs
  - Parallelism-agnostic

- Supports essentially all of C:
  - Complex control flow
e.g., goto, switch, function calls
  - Arbitrary memory structures
e.g., pointers, structs, stack, heap
  - Arbitrary operators
e.g., floating point, divide
  - Memory coherent with host CPU

```c
sumArray(int *a, int n)
{
    int i = 0;
    int sum = 0;

    for (i = 0; i < n; i++) {
        sum += a[i];
    }

    return sum;
}
```
Constructing a C-core

- **Compilation**
  - C-core selection
  - SSA, infinite register, 3-address code
  - Direct mapping from CFG and DFG
  - Scan chain insertion

- **Verilog → Synthesis, P&R**
  - 45 nm process
  - Synopsys CAD flow
    - Synthesis
    - Placement
    - Clock tree generation
    - Routing

Image: Diagram of a circuit with labels for scan chain, data path, control path, cache interface, and circuit metrics of 0.01 mm², 1.4 GHz.
C-cores Experimental Data

- We automatically built 21 c-cores for 9 "hard" applications

  - 45 nm TSMC
  - Vary in size from 0.10 to 0.25 mm²
  - Frequencies from 1.0 to 1.4 GHz

<table>
<thead>
<tr>
<th>Application</th>
<th># C-cores</th>
<th>Area (mm²)</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>bzip2</td>
<td>1</td>
<td>0.18</td>
<td>1235</td>
</tr>
<tr>
<td>cjpeg</td>
<td>3</td>
<td>0.18</td>
<td>1451</td>
</tr>
<tr>
<td>djpeg</td>
<td>3</td>
<td>0.21</td>
<td>1460</td>
</tr>
<tr>
<td>mcf</td>
<td>3</td>
<td>0.17</td>
<td>1407</td>
</tr>
<tr>
<td>radix</td>
<td>1</td>
<td>0.10</td>
<td>1364</td>
</tr>
<tr>
<td>sat solver</td>
<td>2</td>
<td>0.20</td>
<td>1275</td>
</tr>
<tr>
<td>twolf</td>
<td>6</td>
<td>0.25</td>
<td>1426</td>
</tr>
<tr>
<td>viterbi</td>
<td>1</td>
<td>0.12</td>
<td>1264</td>
</tr>
<tr>
<td>vpr</td>
<td>1</td>
<td>0.24</td>
<td>1074</td>
</tr>
</tbody>
</table>
C-core Energy Efficiency: Non-cache Operations

- Up to 18x more energy-efficient (13.7x on average), compared to running on an efficient MIPS processor
- Performance is also better (e.g. 1.3x)
Where do the energy savings come from?

MIPS baseline 91 pJ/instr.

C-cores 8 pJ/instr.
Supporting Software Changes

- Software may change – HW must remain usable
  - C-cores unaffected by changes to cold regions
- Can support any changes, through patching
  - Arbitrary insertion of code – software exception mechanism
  - Changes to program constants – configurable registers
  - Changes to operators – configurable functional units
- Software exception mechanism
  - Scan in values from c-core
  - Execute in processor
  - Scan out values back to c-core to resume execution
Patchability Payoff: Longevity

- **Graceful degradation**
  - Lower initial efficiency
  - Much longer useful lifetime

- **Increased viability**
  - With patching, utility lasts ~10 years for 4 out of 5 applications
  - Decreases risks of specialization
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The GreenDroid Mobile Application Processor
Mobile Application Processors Face the Utilization Wall

- The evolution of mobile application processors mirrors that of microprocessors

- Application processors face the utilization wall
  - Growing performance demands
  - Extreme energy/power constraints (mostly battery)
Android™

- Google’s OS + app. environment for mobile devices
- Java applications run on the Dalvik virtual machine
- Apps share a set of libraries (libc, OpenGL, SQLite, etc.)
Applying C-cores to Android

- Android is well-suited for c-cores
  - Core set of commonly used applications
  - Libraries are hot code
  - Dalvik virtual machine is hot code
  - Libraries, Dalvik, and kernel & application hotspots → c-cores
  - Relatively short hardware replacement cycle
Android Workload Profile

- Profiled common Android apps to find the hot spots, including:
  - Google: Browser, Gallery, Mail, Maps, Music, Video
  - Pandora
  - Photoshop Mobile
  - Robo Defense game

- Broad-based c-cores
  - 72% code sharing

- Targeted c-cores
  - 95% coverage with just 43,000 static instructions (approx. 7 mm²)
GreenDroid: Using c-cores to reduce energy in mobile application processors

GreenDroid Tiled Architecture

- Tiled lattice of 16 cores
  (arch. scalability)
- Each tile contains
  - 6-10 Android c-cores
    (~125 total)
  - 32 KB D-cache
    (shared with CPU)
  - MIPS processor
    - 32 bit, in-order, 7-stage pipeline
    - 16 KB I-cache
    - Single-precision FPU
  - On-chip network router
GreenDroid: Energy per Instruction

- More area dedicated to c-cores yields higher execution coverage and lower energy per instruction (EPI)

- 7 mm$^2$ of c-cores provides:
  - 95% execution coverage
  - 8x energy savings over MIPS core
What kinds of hotspots turn into GreenDroid c-cores?

<table>
<thead>
<tr>
<th>C-core</th>
<th>Library</th>
<th># Apps</th>
<th>Coverage (est., %)</th>
<th>Area (est., mm²)</th>
<th>Broad-based</th>
</tr>
</thead>
<tbody>
<tr>
<td>dvmInterpretStd</td>
<td>libdvm</td>
<td>8</td>
<td>10.8</td>
<td>0.414</td>
<td>Y</td>
</tr>
<tr>
<td>scanObject</td>
<td>libdvm</td>
<td>8</td>
<td>3.6</td>
<td>0.061</td>
<td>Y</td>
</tr>
<tr>
<td>S32A_D565_Opaque_Dither</td>
<td>libskia</td>
<td>8</td>
<td>2.8</td>
<td>0.014</td>
<td>Y</td>
</tr>
<tr>
<td>src_aligned</td>
<td>libc</td>
<td>8</td>
<td>2.3</td>
<td>0.005</td>
<td>Y</td>
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<tr>
<td>S32_opaque_D32_filter_DX DY</td>
<td>libskia</td>
<td>1</td>
<td>2.2</td>
<td>0.013</td>
<td>N</td>
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<tr>
<td>less_than_32_left</td>
<td>libc</td>
<td>7</td>
<td>1.7</td>
<td>0.013</td>
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<tr>
<td>cached_aligned32</td>
<td>libc</td>
<td>9</td>
<td>1.5</td>
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<tr>
<td>.plt</td>
<td>&lt;many&gt;</td>
<td>8</td>
<td>1.4</td>
<td>0.043</td>
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<tr>
<td>memcpy</td>
<td>libc</td>
<td>8</td>
<td>1.2</td>
<td>0.003</td>
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<td>1.2</td>
<td>0.005</td>
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<td>0.015</td>
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<td>DiagonalInterpMC</td>
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<td>libz</td>
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<td>0.9</td>
<td>0.055</td>
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# GreenDroid: Projected Energy

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<th>Configuration</th>
<th>Energy (pJ/instr)</th>
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<tr>
<td>Aggressive mobile application processor</td>
<td>91</td>
</tr>
<tr>
<td>(45 nm, 1.5 GHz)</td>
<td></td>
</tr>
<tr>
<td>GreenDroid c-cores</td>
<td>8</td>
</tr>
<tr>
<td>GreenDroid c-cores + cold code (est.)</td>
<td>12</td>
</tr>
</tbody>
</table>

- GreenDroid c-cores use 11x less energy per instruction than an aggressive mobile application processor
- Including cold code, GreenDroid will still save ~7.5x energy
Conclusions

- The utilization wall leads to exponential worsening of the dark silicon problem and forces us to change how we build processors.

- Conservation cores use dark silicon to attack the utilization wall by reducing energy across all hot code, including irregular code.

- GreenDroid will demonstrate the benefits of c-cores for mobile application processors.

- We are developing GreenDroid, a 45 nm tiled prototype, at UCSD.
For the details:


- Efficient Complex Operators for Irregular Codes, HPCA 2011.


greendroid.org