Ling Zhang

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Research/Work interests

- Clock network distribution, clock skew analysis
- High speed on-chip/off-chip interconnect design
- Interconnect equalization, low power design
- Routing and placement algorithm

Education

- PhD candidate, CSE Dept. University of California, San Diego, Sept. 2007-present
- PhD student of VLSI Lab, CSE Dept. University of California, San Diego, Sept. 2004-Sept. 2007
  GPA: 3.92/4.00
- Master of Engineering in Computer Science and Engineering, Tsinghua University, Beijing, China, Sept 2002-Jul. 2004
  GPA: 87.3/100
- Bachelor of Engineering in Microelectronics, Tsinghua University, Beijing, China, Sept. 1998-Jul. 2002
  GPA: 87.7/100
- Minor Degree in English Language, Tsinghua University, Beijing, China, Sept. 1998-Jul. 2002

Research Experience

- Internship, clock synthesis group in Synopsys, Inc, Mountain View, San Jose, Jun – Sept. 2006
  Clock mesh synthesis and distribution algorithm development.
- Internship, EDA Lab in NEC Corporation, Kawasaki, Japan, Jun. 2005-Aug. 2005
  Clock planning system and link insertion algorithms development considering process variations.
- Research assistant, CSE Dept. University of California, San Diego, Sept. 2004-present
  On-chip and off-chip interconnect analysis and optimization, clock network analysis.
  Supervisor: Professor Chung-Kuan Cheng
- Research assistant, EDA Lab in CSE Dept. Tsinghua Univ., Beijing, China, Sept. 2002-Jul. 2004
  Standard cell global routing algorithms, crosstalk estimation and reduction in global routing.
  Supervisor: Professor Tong Jing
- Research assistant, CAD Lab in the Institute of Microelectronics, Tsinghua University, Beijing, China, Jun. 2001-Jun. 2002
  Development of a computer aided manufacture software for silicon wafer manufacture.
- Research assistant, IC Design Lab in the Institute of Microelectronics, Tsinghua University, Beijing, China, Jul. 2000-Sept. 2001
  Logic design, logic verification, circuit simulation, layout design, and post simulation of a Serial Code Generator circuit.

Skills

- EDA tools: IC compiler, Hspice, CosmosScope, PowerSpice, EIP, Xilinx ISE.
- Programming Language: C, Verilog, Perl, Matlab.
- Software tools: Purify, Quantify, ClearCase
- Operating System: Linux, Windows.

Publications

- **L. Zhang**, W. Yu, Y. Zhang, R. Wang, A. Deutsch, G. A. Katopis, D. M. Dreps, J. Buckwalter, E. Kuh, C-K Cheng, Low Power Passive Equalization Design for Computer Memory Links. In: *Proceedings of IEEE Symposium on High-Performance Interconnects*, 2008
- Y. Zhang, **L. Zhang**, A. Tsuchiya, M. Hashimoto, C-K Cheng, On-chip High Performance Signaling Using Passive Compensation. *To appear in Proceedings of IEEE ICCD, 2008*
- Y. Zhang, **L. Zhang**, A. Deutsch, G. A. Katopis, D. M. Dreps, E. Kuh, C-K Cheng, On-chip Bus Signaling Using Passive Compensation. *To appear in Proceedings of IEEE EPEP, 2008*
- **L. Zhang**, W. Yu, H. Zhu, A. Deutsch, G. A. Katopis, D. M. Dreps, E. Kuh, C-K Cheng, Low Power Passive Equalizer Optimization Using Tritonic Step Response. In: *Proceedings of IEEE/ACM DAC*, 2008
- **L. Zhang**, W. Yu, H. Zhu, C-K Cheng, Clock Skew Analysis via Vector Fitting in Frequency Domain. In: *Proceedings of IEEE ISQED*, 2008
- **L. Zhang**, H. Zhu, J. Liu, C-K Cheng, High Performance Current-Mode Differential Logic. In: Proceedings of *IEEE/ACM ASP-DAC*, 2008
- W. Zhang**,** Y. Zhu, W. Yu**, L. Zhang,** R. Shi, H. Peng, Z. Zhu, L. Chua-Eoan, R. Murgai, T. Shibuya, N. Ito, C-K Cheng. Finding the Worst Voltage Violation in Multi-Domain Clock Gated Power Network. In: *Proceedings of IEEE DATE*, 2008.
- **L. Zhang**, H. Chen, B. Yao, K. Hamilton, C-K Cheng. Repeated On-Chip Interconnect Analysis and Evaluation of Delay, Power, and Bandwidth Metrics under Different Design Goals. In: *Proceedings of IEEE ISQED*, 2007
- W. Zhang**, L. Zhang,** R. Shi, H. Peng, Z. Zhu, L. Chua-Eoan, R. Murgai, T. Shibuya, N. Ito, C-K Cheng. Fast Power Network Analysis with Multiple Clock Domains. In: *Proceedings of IEEE ICCD*, 2007
- T. Jing, **L. Zhang**, J. Liang, J. Xu, X. Hong, J. Xiong, L. He. A Min-area Solution to Performance and RLC Crosstalk Driven Global Routing Problem. In: *Proceedings of IEEE/ACM ASP-DAC*, 2005.
- **L. Zhang**, T. Jing, X. Hong, J. Xu, L. He, J. Xiong. Performance Optimization Global Routing with RLC Crosstalk Constraints. In: *Proceedings of IEEE ASICON*, 2003. **Outstanding student paper award**
- **L. Zhang**, T. Jing, X. Hong, C. Yang, M. Shen. GUI Design Based on Registration Mechanism for Data-Path Layout. *Computer Engineering and Applications*, 2003.
- **L. Zhang**, T. Jing, X. Hong, J. Xu, J. Xiong, L. He. Performance and RLC Crosstalk Driven Global Routing. In: *Proceedings of IEEE ISCAS*, 2004.
- **L. Zhang**, T. Jing, X. Hong, J. Xu, J. Xiong, L. He. CEE-Gr: A Global Router with Performance Optimization under Multi-Constraints. *Chinese Journal of Semiconductors*, 2004.

Awards

- First runner-up for Research-Expo of UCSD, CSE Dept. 2007.
- Tsinghua Scholarship for excellent graduate student, 2002-2003
- Outstanding Student Paper Award of *the 5th IEEE international conference on ASIC* (*IEEE ASICON 2003*)
- Outstanding Graduate of EE Dept, Tsinghua University, 2002 (10/60)
- Tsinghua Scholarship of Excellence, 98-99, 99-00,00-01 respectively (10/250)
- Tsinghua Scholarship of Excellent Freshmen, 1998 (10/250)