Placement and Beyond in Honor of Ernest S. Kuh

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Placement and Beyond

• Ernest S. Kuh is a pioneer and giant in physical layout.
• C&C Prize, Japan Society for Promotion of Communication and Computers, 1996.
• EDAA Lifetime Achievement Award, 2008
• Robert Gustav Kirchhoff Award, 2009
Outlines

• Placement
• Applications
• Team
• Second Waves
• Scaling and Trends
Placement

• 1-D Gate Assignment: Interval Graph
• Building Block Layout: BBL, BEAR
• Gate Array Layout: BAGEL
• Standard Cell Placement: RAMP, PROUD
• Performance Driven Placement: Congestion, Timing, Low Power
Placement

- Productivity: Theory, Software Package, Application
- Core of Physical Synthesis: > $500 Millions Market
Building Block Layout

• Issues: Representation, Routability
• Nonslicing Architecture
  – Representation: Tile Plane
  – Routability: Routing Order for 100% routing completion
• Applications
  – Digital Equipment Corporation
  – ECAD, Cadence
Standard Cell Placement

• Issues: Complexity, Timing Convergence due to Interconnect Dominance

• RAMP, PROUD
  – Analogy of a resistive network
  – Quadratic wire length minimization

• Analytical vs. Iterative Approaches
  – Quadratic Programming
  – Simulated Annealing (‘83 Kirkpatrick)

• Applications
  – Qplacer
Analytical Placement

- Quinn and Breuer, 1979: Force Model
  - Hook’s law for attraction
  - Repulsive force for pairs without connection
- Antreich, Johannes, and Kirsh, 1982: Systematic Formulation
- RAMP, 1983: Delete repulsive force
  - Sparse matrix operations
- GALA, 1984: Gate Array Layout, Hughes Aircraft Comp.
- PROUD, 1988: Successive Over Relaxation
- Qplacer, 1992: Louis Chao, Cadence
- R.S. Tsay, 1992: Avanti, Synopsys
- Eisenmann and Johannes, 1998:
- Naylor, Donelly, Sha, 2001: Nonlinear function for hyperlinks, Synopsys
Application

• 1983, Hughes: 104 seconds, 1 MIPs, 136 modules
• 1991, Kleinhans et al.: 2500 seconds, 15 MIPs, 6417 modules
• 1998, Eisenmann and Johannes: 2031 seconds, AlphaStation (266 MHz), 25K modules
• Present: 6-7M components of 30-40 transistors
Teams

- Building Block Layout: Nang-Ping Chen, Chi-Ping Hsu, Chao-Chiang Chen, Wayne Dai, Bernhard Eschermann, Massoud Pedram, Yasushi Ogawa, and Margaret Sadowska
- Channel ordering scheme for the layout: Wayne Dai and Tetsuo Asano
- Gate array layout: Margaret Sadowska, Jeong-Tyng Li and C.K. Cheng
- Standard placement: C.K. Cheng, Ren-Song Tsay
- Low power placement: Massoud Pedram
- Timing driven placement: Shen Lin, Srinivasan Arvind, Michael Jackson, Henrik Esbensen, and Margaret Sadowska
- IO assignment: Massoud Pedram, Narasimha Bhat, Kamal Chaudhary, Deborah Wang, and Margaret Sadowska
- Gate matrix layout: Dong-Min Xu
- Partitioning: Minshine Shih
- Floorplan: Pinhong Chen, Hiroshi Murata
Second Waves

- Prof. Hidoshi Onodera, Kyoto University: building block placement, 1991
- Prof. Xianlong Hong, Tsinghua University: floorplan representation, corner block list, 2000
- Prof. John Lillis, University of Illinois, Chicago: placement tool, Mongrel using hybrid techniques for standard cell placement, 2000
- Prof. Andrew B. Kahng, UC San Diego: APlacer which won ACM International Symposium on Physical Design placement contest, 2005
Scaling and Trends

Optimal Solution or Error Bound?

• Steinberg, 1961: 34 modules
• Stevens, 1972: 67-151 modules
• Hughes, 1983: 300-500 modules
• MCNC, 1991: 15K modules
Scaling and Trends

Geometry Handling, Combinatorial Algorithms, Circuit Performance, and Advancement of Technologies

- Mixed module placement
- Placement of heterogeneous circuits
- Placement integrating behavior synthesis
- 3-D Placement
- Parallel Placement
Placement and Beyond

• Basic Circuit Theory, 1969
  – Charles A. Desoer and Ernest S. Kuh
• SPICE, 1971
  – Ronald A. Rohrer and Donald O. Pederson
• SWEC, 1991: Recursive Convolution
  – Shen Lin and Margaret Sadowska
• Transmission Line, 1999: Model Order Reduction
  – Janet Wang and Qingjian Yu
• Circuit Simulation, 2005-2009: Parallel SPICE
THANK YOU