Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator

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• Introduction
• Architecture of On-Chip Global Link
• Receiver: Comparator and Latch
• Transmission-line
• Driver: CTLE and LVDS
• Simulation Results
• Conclusion
Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator

Introduction
Introduction

On-Chip Interconnect Issues (45nm node)

- Power: \(~0.2\text{pJ/mm/b}\)
- Delay: \(~70\text{ps/mm}\)
- Throughput: \(~10\text{Gbp/um}\)
- Current Density
Goal

• Ultra-low power on chip interconnection
• Ultra-low power high resolution comparator
• LTE-combined LVDS buffer
• Model as PTM 64 nm LVT
• 1.1V, 0.8v split power supply
• 10 GHz, top Layer 10mm/intermediate layer 2.5mm connection
• FOM ~20fJ/mm/b
• Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator

Architecture of On-Chip Global Link
• **Architecture of On-Chip Global Link**

Main Components:
• Driver: CTLE combined LVDS
  • shared-components and save power
• Receiver: Sense-amplifier and latches
  • shared-components and save power
• T-line model for on-chip interconnection
• **Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator**

Receiver: Comparator and Latch
• Receiver: Comparator and Latch

Working Principle:
• No Miller effect from sense amplifier stage to latches. Speed bottleneck is not pre-amplifier anymore.
• Components reuse, Mn1 & Mn2 (as load for sense-amplifier and NMOS for latches)
• Current drive instead of voltage drive for latches.
Receiver: Comparator and Latch (Sensitivity)

Pre-amplifying stage:
- Bias current: Mp3. Size of Mp3 with Vbias, provide 140uA bias current.
- Input stage: PMOS input to provide differential current input to next stage. PMOS input could adjust Vbulk to cancel the offset Voltage
- Active load: current path to make sure the input stage in saturation region
- Reset switch: Mp8, reset the drain of Mn1 & Mn2 to the same level

Fig.3. Comparator in a. CK=0 and b. CK=1 cases
Pre-amplifying stage:
- The minimum detect current within 50ps, 5mv offset is 100nA
- Sense amplifier provide the differential current directly to speed up the circuits
Receiver: Comparator and Latch (Small Signal Model)

AC analysis when differential input is very small

Fig.4. Small signal analysis when in CK=Vdd

\[
\begin{align*}
\text{Voltage Loop-Gain:} & \quad + \left( g_{m_n} + g_{m_p} \right)^2 \cdot \left( r_n // r_p \right)^2 \\
R_{in} & = \frac{\left( r_n // r_p \right) \cdot \left( r_n // r_p \right)^2}{1 - \left( g_{m_n} + g_{m_p} \right)^2 \cdot \left( r_n // r_p \right)^2} \\
& = \frac{1}{1 - \left( g_{m_n} + g_{m_p} \right) \cdot (g_{m_n} + g_{m_p}) \cdot (r_n // r_p)} \\
& = \frac{1}{-\left( g_{m_n} + g_{m_p} \right) \cdot (g_{m_n} + g_{m_p})} \cdot \frac{1}{\text{Intrinsic gain}} \\
\text{Initiate Amplitude:} & \quad \Delta V = R_{in} \cdot \Delta I \\
\text{Time constant:} & \quad \tau = R_{in} \cdot C_{parasitic}
\end{align*}
\]
Comparator: optimization & Power consumption

Fig.6. Output of Comparator with input voltage from 2mv to 256 mv

Fig.7. Output of Comparator with latch transistor size from 1 to 32

Fig.8. Output voltage with size of pre-amplifier input pairs from 20 to 120

Fig.9. Current consumption on 1.1v supply with 4mv input
• Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator

Transmission-line
• **Design and Modeling Transmission-line**

Intermediate layer interconnect T-Line model for 1000x2.5um

\[
\begin{align*}
W &= 0.5\text{um} \\
s &= 0.5\text{um} \\
l &= 2.5\text{um} \\
t &= 0.35\text{um} \\
h &= 0.2\text{um} \\
K &= 2.2
\end{align*}
\]

\[
\begin{align*}
R_{\text{gnd}} &= 0.045\text{Ohm} \\
L_{\text{gnd}} &= 0.0015\text{nH} \\
R_{T-\text{line}} &= 0.314\text{Ohm} \\
L_{T-\text{line}} &= 0.0022\text{nH}
\end{align*}
\]

\[
C_{\text{gnd}} = 0.1860525\text{fF} \\
C_{\text{couple}} = 0.02409\text{fF} \\
K_{\text{sig-gnd}} = 0.5
\]

Fig.10. Intermediate layer model and its parameter in 45nm technology

View 1: use 2.5um model in series with one another for 1000 times

View 2: use TSMC 65nm process Cadence Virtuoso to extra RLC model for the post-layout simulation, to get the almost similar results.

Fig.11. RLC equivalent circuits model for top layer

Layout:
• TSMC65nm Process
• Cadence Virtuoso
• RLC Extra to the post-layout model
• **Design and Modeling Transmission-line**

Advanced modeling for T-Line model for 1000x2.5um

- T-line Model is improved to more practical one. Only shield wires in the same layer are there. The top layer and bottom layer are used by the other signals orthogonal to desired signal.

- With IBM EIP tool, the noise source from Metal 7 and Metal 3 is more than -20dB.

- Differential T-line is shielded by one layer up and one layer down as well as the side wire to get the better noise performance.

\[
R_{\text{ground}} = 0.045 \text{Ohm} \\
L_{\text{ground}} = 0.0015 \text{nH} \\
R_{T-\text{line}} = 0.314 \text{Ohm} \\
L_{T-\text{line}} = 0.0022 \text{nH}
\]

\[
C_{\text{ground}} = 0.1860525 \text{fF} \\
C_{\text{couple}} = 0.02409 \text{fF} \quad K_{\text{signal-ground}} = 0.5
\]
- **Ultra-Low Power On-Chip Differential Interconnects Using High-Resolution Comparator**

Driver: CTLE + LVDS Buffer
CTLE combined LVDS to save power

\[ R_s = \frac{R_{CTLE}}{2} \]  
\[ C_s = 2C_{CTLE} + C_{par\text{-}mp5} \]  
\[ R_D = r_{ds2} \parallel R_{T\text{-line}\text{-eq}} \]  
\[ C_p = C_{T\text{-line}\text{-eq}} \]  
\[ \omega_2 = \frac{1}{R_s C_s} \]  
\[ \omega_{p1} = \frac{1 + g_m R_s}{2 R_s C_s} \]  
\[ \omega_{p2} = \frac{1}{R_D C_p} \]  
DC gain = \frac{g_m R_D}{1 + g_m R_s / 2}  
Ideal peak gain = g_m R_D  
Ideal Peaking = \frac{\omega_{p1}}{\omega_2} = 1 + g_m R_s / 2  
DC gain = g_m R_D
Simulation Results & Conclusion
• Simulation Results

Table 1. Performance comparison

Fig. 14. Eye-Diagram of T-line input and comparator input

Fig. 15. Current and power consumption in driver stage and receiver stage
## Simulation Results

<table>
<thead>
<tr>
<th>Metrics</th>
<th>state of art [1]</th>
<th>work-a</th>
<th>work-b</th>
<th>work-c</th>
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<tbody>
<tr>
<td>Total Power (mw)</td>
<td>3.91</td>
<td>0.534</td>
<td>0.481</td>
<td>0.435</td>
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<tr>
<td>driver (mw)</td>
<td>1.88</td>
<td>0.345</td>
<td>0.292</td>
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<td>receiver (mw)</td>
<td>2.03</td>
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<td>0.189</td>
<td>0.189</td>
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<tr>
<td>Energy/bit (pJ/b)</td>
<td>0.196</td>
<td>0.053</td>
<td>0.048</td>
<td>0.044</td>
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<tr>
<td>Total Delay (ps)</td>
<td>110</td>
<td>215</td>
<td>138</td>
<td>149</td>
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<tr>
<td>driver (ps)</td>
<td>30</td>
<td>20</td>
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<td>28</td>
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<tr>
<td>T-line (ps)</td>
<td>80</td>
<td>105</td>
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<tr>
<td>receiver (ps)</td>
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<tr>
<td>Delay/length(ps/mm)</td>
<td>14.5</td>
<td>21.5</td>
<td>55.2</td>
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<tr>
<td>Bit rate (Gbps)</td>
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<td>10</td>
<td>10</td>
<td>10</td>
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<td>Split-supply</td>
<td>Split-Supply</td>
<td>Split-Supply</td>
</tr>
<tr>
<td>Pitch (um)</td>
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<td>2.2</td>
<td>1.0</td>
<td>0.6</td>
</tr>
<tr>
<td>Wire length (mm)</td>
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<td>10</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Layer</td>
<td>Top</td>
<td>Top</td>
<td>Inter-mediate</td>
<td>Inter-mediate</td>
</tr>
</tbody>
</table>

Table 1. Performance comparison
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Thank you!