

Interests

Architectural enhancements to multi-core memory systems to accelerate and extend support for parallel software constructs and richer memory semantics.

Memory system designs that leverage a decoupling of connectivity and concurrency in extremely heterogeneous CMPs.

Selected Work

Filter Barriers

Developed *filter barriers*, a barrier mechanism specifically designed to be integrated with the existing shared memory systems of CMPs, and showed how fast barrier synchronization improves CMPs as platforms for fine-grained data parallelism [1].

Education

Fall 2003 – Present: University of California, San Diego.

Seeking Ph. D. in Computer Engineering. Expected to graduate in 2010

Thesis topic: **Memory Systems for Massively-heterogeneous CMPs**

C. Phil. in Computer Engineering – Winter 2008

Fall 1998 – Spring 2002: University of California, Berkeley.

B.S. in Electrical Engineering and Computer Science

Work Experience

Summer 2006: Intern, HP Labs, Palo Alto.

Explored performance potential of HW/SW-hybrid transactional memory systems

Summer 2005: Intern, HP Labs, Palo Alto.

Developed multi-core oriented barrier mechanisms to improve the profitability of fine-grain data parallelism on CMPs

Teaching

University of California, San Diego - Teaching Assistant

CSE 141/141L - Computer Architecture/Computer Architecture Lab (Spring 2006)

University of California, Berkeley - Head Teaching Assistant

Computer Science 150 - Components and Design Techniques for Digital Systems (Fall 2002 - Spring 2003)

University of California, Berkeley - Teaching Assistant

Computer Science 150 - Components and Design Techniques for Digital Systems (Spring 2002)

Computer Science 61C - Machine Structures (Fall 2001)

Computer Science 61B - Data Structures (Summer 2000, Fall 2000, Summer 2002)

Talks

Exploiting Fine-Grained Data Parallelism with Chip Multiprocessors and Fast Barriers. *International Symposium on Microarchitecture (MICRO)*, December 2006.

The Strong Correlation Between Code Signatures and Performance. *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2005

Publications

- [1] Jack Sampson, Ruben Gonzalez, Jean-Francois Collard, Norman P. Jouppi, Mike Schlansker, and Brad Calder. Exploiting fine-grained data parallelism with chip multiprocessors and fast barriers. In *MICRO 39: Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture*, pages 235–246, Washington, DC, USA, 2006. IEEE Computer Society.
- [2] Christophe Lemuët, Jack Sampson, Jean-Francois Collard, and Norm Jouppi. The potential energy efficiency of vector acceleration. In *SC '06: Proceedings of the 2006 ACM/IEEE conference on Supercomputing*, page 77, New York, NY, USA, 2006. ACM.
- [3] Weihaw Chuang, Satish Narayanasamy, Ganesh Venkatesh, Jack Sampson, Michael Van Biesbrouck, Gilles Pokam, Brad Calder, and Osvaldo Colavin. Unbounded page-based transactional memory. In *ASPLOS-XII: Proceedings of the 12th international conference on Architectural support for programming languages and operating systems*, pages 347–358, New York, NY, USA, 2006. ACM.
- [4] E. Perelman, M. Polito, J.-Y. Bouguet, J. Sampson, B. Calder, and C. Dulong. Detecting phases in parallel applications on shared memory architectures. *Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International*, pages 10 pp.–, April 2006.
- [5] L. Eeckhout, J. Sampson, and B. Calder. Exploiting program microarchitecture independent characteristics and phase behavior for reduced benchmark suite simulation. *IEEE Workload Characterization Symposium*, 0:2–12, 2005.
- [6] Jeremy Lau, John Sampson, Erez Perelman, Greg Hamerly, and Brad Calder. The strong correlation between code signatures and performance. In *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2005.