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Research Interests

I am interested in the design and implementation of novel architectures that make use of increasingly plentiful transistor resources to improve the energy-efficiency of executing code and to provide qualitatively new features in support of higher-level language constructs. My recent work has focused on designs that exploit the new trade-offs among area, power, and performance brought about by the growing trend of *dark silicon*. My interests are primarily in the area of computer architecture, but include aspects of compilers and VLSI as they relate to developing and using customizable processors, increasing hardware specialization, implementing aggressive power management techniques, designing energy-efficient circuits, and deploying other means of controlling and exploiting the growth of dark silicon. I am also interested in architectural enhancements to multi-core memory systems to accelerate and extend support for parallel software constructs and richer memory semantics, as well as the design of on-chip memory networks for massively-heterogeneous many-core systems.

Education

Fall 2003 – Fall 2010: **University of California, San Diego.**

Ph. D. in Computer Science(Computer Engineering), 2010

Thesis: **Design and Architecture of Automatically-generated Energy-reducing Coprocessors**

Advisors: Steven Swanson and Michael Bedford Taylor

Fall 1998 – Spring 2002: **University of California, Berkeley.**

B.S. in Electrical Engineering and Computer Sciences

Research Projects

GreenDroid

2010 – present

My colleagues and I are developing a prototype mobile application processor called GreenDroid that leverages *dark silicon* to dramatically reduce energy consumption in smart phones. GreenDroid will incorporate many specialized processors (*Conservation Cores*) targeting key portions of Google's Android smart phone platform and reducing their energy consumption. The first GreenDroid processor prototype will be ready for tape-out in the first half of 2012. [6, 7]

Conservation Cores

2007 – present

I have developed an automated C-to-silicon infrastructure for generating specialized hardware to improve the energy efficiency of mature codebases and to integrate these *conservation cores* into a multiprocessor platform. [4, 1, 5, 2, 8].

Memory Systems for Massively-heterogeneous CMPs

2007 – 2008

I have explored designs for memory networks connecting large numbers of heterogeneous specialized processing elements to a shared memory. This included an exploration of lightweight and energy-efficient mechanisms for handling coherence traffic that optimize for migratory patterns of execution.

Hardware-accelerated Software Transactional Memory

2006 – 2007

I investigated the performance-complexity trade-offs of software transactional memory systems accelerated through HW primitives for in-cache meta-data manipulation compared to full-hardware and full-software transactional memory systems.

Filter Barriers

2005 – 2006

I developed *filter barriers*, a barrier mechanism specifically designed to be integrated with the existing shared memory systems of CMPs, and showed how fast barrier synchronization improves CMPs as platforms for fine-grained data parallelism [3].

Program Phase Analysis

2004 – 2005

I worked with my colleagues to extend Simpoint techniques to x86 platforms. I showed how to augment performance counter sampling techniques with static analysis to generate accurate performance predictions from coarse sampling traces. [11].

Refereed Journal and Conference Publications

- [1] Jack Sampson, Manish Arora, Nathan Goulding-Hotta, Ganesh Venkatesh, Jonathan Babb, Vikram Bhatt, Steven Swanson, and Michael Bedford Taylor. An evaluation of selective depipelining for FPGA-based energy-reducing irregular code coprocessors. In *Field Programmable Logic and Applications (FPL), 2011 International Conference on*, pages 24–29. IEEE, 2011.
- [2] Jack Sampson, Ganesh Venkatesh, Nathan Goulding, Saturnino Garcia, Steven Swanson, and Michael Bedford Taylor. Efficient complex operators for irregular codes. In *International Symposium on High-Performance Computer Architecture*, February 2011.
- [3] Jack Sampson, Ruben Gonzalez, Jean-Francois Collard, Norman P. Jouppi, Mike Schlansker, and Brad Calder. Exploiting fine-grained data parallelism with chip multiprocessors and fast barriers. In *MICRO 39: Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture*, pages 235–246, Washington, DC, USA, 2006. IEEE Computer Society.
- [4] Ganesh Venkatesh, Jack Sampson, Nathan Goulding-Hotta, S.K. Venkata, Michael Bedford Taylor, and Steven Swanson. Qscores: Trading dark silicon for scalable energy efficiency with quasi-specific cores. In *Proceedings of the 44th Annual IEEE/ACM International Symposium on Microarchitecture*. IEEE Computer Society, 2011.
- [5] Manish Arora, Jack Sampson, Nathan Goulding-Hotta, Jonathan Babb, Ganesh Venkatesh, Michael Bedford Taylor, and Steven Swanson. Reducing the energy cost of irregular code bases in soft processor systems. In *Field-Programmable Custom Computing Machines (FCCM), 2011 IEEE 19th Annual International Symposium on*, pages 210–213. IEEE, 2011.
- [6] Nathan Goulding-Hotta, Jack Sampson, Ganesh Venkatesh, Saturnino Garcia, Joe Auricchio, P. Huang, Manish Arora, Siddhartha Nath, Vikram Bhatt, Jonathan Babb, Michael Bedford Taylor, and Steven Swanson. The GreenDroid mobile application processor: An architecture for silicon’s dark future. *Micro, IEEE*, 31(2):86–95, 2011.
- [7] Nathan Goulding, Jack Sampson, Ganesh Venkatesh, Saturnino Garcia, Joe Auricchio, Jonathan Babb, Michael Bedford Taylor, and Steven Swanson. GreenDroid: A mobile application processor for a future of dark silicon. *Hot Chips*, 2010.
- [8] Ganesh Venkatesh, Jack Sampson, Nathan Goulding, Saturnino Garcia, Vladyslav Bryksin, Jose Lugo-Martinez, Steven Swanson, and Michael Bedford Taylor. Conservation cores: Reducing the energy of mature computations. In *International Conference on Architectural Support for Programming Languages and Operating Systems*, March 2010.
- [9] Christophe Lemuett, Jack Sampson, Jean-Francois Collard, and Norm Jouppi. The potential energy efficiency of vector acceleration. In *SC '06: Proceedings of the 2006 ACM/IEEE conference on Supercomputing*, page 77, New York, NY, USA, 2006. ACM.
- [10] Lieven Eeckhout, Jack Sampson, and Brad Calder. Exploiting program microarchitecture independent characteristics and phase behavior for reduced benchmark suite simulation. *IEEE Workload Characterization Symposium*, 0:2–12, 2005.
- [11] Jeremy Lau, John Sampson, Erez Perelman, Greg Hamerly, and Brad Calder. The strong correlation between code signatures and performance. In *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2005.
- [12] Vasileios Kontorinis, Liuyi Zhang, Boris Aksanli, Jack Sampson, Houman Homayoun, Edward Pettis, Dean Tullsen, and Tajana Rosing. Managing distributed UPS energy for effective power capping in data centers. In *Proceedings of the 39th Annual International Symposium on Computer Architecture (ISCA)*, June 2012.

- [13] Weihaw Chuang, Satish Narayanasamy, Ganesh Venkatesh, Jack Sampson, Michael Van Biesbrouck, Gilles Pokam, Brad Calder, and Osvaldo Colavin. Unbounded page-based transactional memory. In *ASPLOS-XII: Proceedings of the 12th international conference on Architectural support for programming languages and operating systems*, pages 347–358, New York, NY, USA, 2006. ACM.
- [14] Erez Perelman, Marzia Polito, Jean-Yves Bouguet, Jack Sampson, Brad Calder, and Carole Dulong. Detecting phases in parallel applications on shared memory architectures. *Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International*, April 2006.

Patents

US7587555: Program thread synchronization. Jean-Francois Collard, Norman P. Jouppi, John M Sampson

Teaching and Mentoring Experience

Co-Instructor, *UCSD CSE 291 - Smartphone Processor Design* Fall 2011
Presented background material, led discussions, and provided guidance for a project-oriented, exploratory graduate-level class.

Postdoctoral Scholar, *GreenDroid Group* 2010 – present
Research mentor for junior graduate students. Oversaw a first year student’s development of a presentation and poster for FCCM. Ran group meetings on occasions when the principle investigators were unavailable.

Teaching Assistant, *UCSD CSE 141 - Computer Architecture* Spring 2006

Teaching Assistant, *UCSD CSE 141L - Computer Architecture Lab* Spring 2006
Alternated leading of weekly discussion section with other TA. Held office hours, extensive lab hours, and graded assignments and labs.

Head Teaching Assistant, *UC Berkeley CS 150 - Digital Design* Fall 2002 – Spring 2003
In addition to regular TA duties (as below), I generated the weekly in-class quizzes, developed new project support infrastructure, and gave lectures on two occasions when the professor was unavailable.

Teaching Assistant, *UC Berkeley CS 150 - Digital Design* Spring 2002

Teaching Assistant, *UC Berkeley CS 61C - Machine Structures* Fall 2001

Teaching Assistant, *UC Berkeley CS 61B - Data Structures* Summer 2000, Fall 2000, Summer 2002
Led weekly or twice-weekly discussion sections, held lab hours, held office hours, graded labs and assisted in running review sessions and the grading of exams and quizzes.

Conference Talks and Presentations

An Evaluation of Selective Depipelining for FPGA-based Energy-Reducing Irregular Code Coprocessors. *International Conference on Field Programmable Logic and Applications (FPL)*, September, 2011.

Efficient Complex Operators for Irregular Codes. *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2011.

Conservation Cores: Reducing the Energy of Mature Computations. *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2010.

Exploiting Fine-Grained Data Parallelism with Chip Multiprocessors and Fast Barriers. *International Symposium on Microarchitecture (MICRO)*, December 2006.

The Strong Correlation Between Code Signatures and Performance. *International Symposium on Performance Analysis of Systems and Software (ISPASS)*, March 2005.

Work Experience

- University of California, San Diego, *Postdoctoral Scholar*** 2010-Present
I am currently part of the GreenDroid group, which is producing a prototype mobile applications processor for Android using Conservation Cores.
- HP Labs, Palo Alto, *Intern*** Summer 2006
During this internship, I explored the performance potential of HW/SW-hybrid transactional memory systems.
- HP Labs, Palo Alto, *Intern*** Summer 2005
During this internship, I developed multi-core oriented barrier mechanisms to improve the profitability of fine-grain data parallelism on CMPs, and examined the energy efficiency of vector architectures.
- University of California, San Diego, *Research Assistant*** 2004-2010
As a graduate student researcher, I worked in the area of computer architecture.

Misc

Organizer for *DaSi*, the Dark Silicon workshop.

References

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