HIGH THROUGHPUT CHANNEL TRACKING FOR JTRS WIRELESS CHANNEL EMULATOR

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MOTIVATION - CHANNEL EMULATOR
- A virtual platform to simulate radio environment to test and verify wireless system in laboratory

PROBLEMS
- Performance & Scalability
- Unknown frequency hopping techniques over a range of 250 MHz bandwidth

SYSTEM OVERVIEW
- Highly scalable JTRS channel emulator network (up to 1000)
- Real-time channel tracker spanning frequency hopping
- HLS optimization methodologies

SYSTEM SPECIFICATION
- Pentek Cobalt board
  - Xilinx Vertex 6 series FPGA (XC6VSX315TFF1156-2)
  - 500 MHz ADCs & DDCs
  - 800 MHz DACs & DUCs
  - PCI Express Interface to communicate to a host PC
- Xilinx Vivado HLS 2012.3
- Xilinx ISE 12.4

HLS OPTIMIZATION STRATEGY
- Single threaded implementation
- If conditions and parameters nested
- Strong data dependency

CONTRIBUTIONS
- Tracking intermediate frequency signals in 250 MHz
- Detecting the carrier signal of 51 frequency slots
- Analyzing signal spectrum based on linear prediction
- Generating a programmable DDC module control signal

LATENCY VS THROUGHPUT
- Concurrent functional modules
- Minimum functional dependency

LATENCY VS THROUGHPUT

RESULTS

Performance in different designs

The size of input samples

Pattern of throughput

Resource usage

Module throughputs

Module a

Module b

Module c

Input buffering

Output buffering

Throughput Optimization

Latency (cycles)

Area usage (%)

SLICE 940 (2%)

LUTs 2104 (1%)

FFs 2338 (0.5%)

DSPs 112 (0.3%)

BRAMs 3 (0.2%)

Total latency 71

Modular architecture

Highly scalable JTRS channel emulator network for JTRS wireless channel emulator