1. Enumerate the data hazards and give an example for each.
   
a. RAW (Read after Write)
   
   \[ \text{ADD } R1, R2, R3 \]
   \[ \text{ADD } R4, R1, R5 \]
   
b. WAW (Write after Write)
   
   \[ \text{ADD } R1, R2, R3 \]
   \[ \text{ADD } R1, R4, R5 \]
   
c. WAR (Write after Read)
   
   \[ \text{ADD } R1, R2, R3 \]
   \[ \text{ADD } R2, R4, R5 \]

2. Show the pipeline register for your 2-stage processor and enumerate what information is stored in the pipeline register.
   
a. Register file’s write enable (regWrEn)
   b. Memory’s write enable (memWrEn)
   c. Multiplexers’ select generated by the controller (mulSel)
   d. Alu’s result (aluOut)
   e. Program counter (PC)
   f. Instruction type (e.g. branch, JAL)
   g. Branch Taken/Not Taken