

# Chengmo Yang

CSE Department, UC San Diego  
La Jolla, CA 92093-0404  
Tel: 858-822-2505, E-mail: [c5yang@cs.ucsd.edu](mailto:c5yang@cs.ucsd.edu)  
Web: [www.cs.ucsd.edu/~c5yang](http://www.cs.ucsd.edu/~c5yang)

## **Research Interests:**

Execution adaptivity in multicore systems, fault-tolerant multiprocessor and processor architectures, power- and thermal-aware system design, adaptive task scheduling and resource management, efficient on-chip communication and synchronization schemes

## **Ph.D. Thesis:**

Fine-grained and Predictable Execution Adaptivity in Advanced Multicore Systems

## **Education:**

- **Ph.D.** Computer Engineering UC San Diego 2003-present GPA: 3.93/4.0
- **M.S.** Computer Science UC San Diego 2003-2005 GPA: 3.93/4.0
- **B.S.** Microelectronics Peking University, China 1999-2003 GPA: 3.79/4.0

## **Honors and Awards:**

- Samsung Scholarship in Peking University, October 2002 (only top 3% eligible)
- Dongshi Scholarship in Peking University, October 2001 (only top 3% eligible)
- Guangcai Scholarship in Peking University, October 2000 (only top 3% eligible)

## **Research Experience:**

*Research Assistant (2004-present)*, at ART (Architecture, Reliability, Testing) group, UC San Diego

- Reconfigurable and adaptive task scheduling and optimization for MPSoCs
- Cache-based fault detection techniques for multiprocessors
- Light-weight synchronization for on-chip communications
- Power-efficient branch prediction and instruction delivery techniques

*Research Study (2002-2003)*, at MPRC (Microprocessor Research & Development Center), Peking University, China

- Instruction-level simulation & verification for SoCs
- Logic synthesis & static timing analysis for SoCs

## **Teaching Experience:**

*Teaching Assistant (2009, 2008, 2007, 2005, 2004)*, at UC San Diego for

- CSE 240A: “Principles in Computer Architecture”
- CSE 141: “Introduction to Computer Architecture”
- CSE 120: “Principles of Computer Operating Systems”
- CSE 140: “Components and Design Techniques for Digital Systems”
- CSE 140L: “Digital Systems Laboratory”

## **Industry Experience:**

**Engineer Intern** (Summer 2008, Summer 2007), at Broadcom Corporation, San Diego, CA

Developing a behavior-level cycle accurate simulation and testing environment based on RTL description of application-specific SoCs.

**Engineer Intern** (Summer 2006), at Mindspeed Technologies, Newport Beach, CA

Developing a cycle accurate configurable system-level simulator for an application-specific SoC for voice processing products.

## **Publications:**

### ***Conference Papers***

- C. Yang, M Chen, and A. Orailoglu, "Squashing Microcode Stores to Size in Embedded Systems while Delivering Rapid Microcode Accesses," in *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, October 2009. **(nominated for best paper)**
- C. Yang and A. Orailoglu, "Processor Reliability Enhancement through Compiler-Directed Register File Peak Temperature Reduction," in *International Conference on Dependable Systems and Networks (DSN)*, June 2009.
- C. Yang and A. Orailoglu, "Towards No-cost Adaptive MPSoC Static Schedules through Exploitation of Logical-to-physical Core Mapping Latitude," in *IEEE Design, Automation and Test in Europe (DATE)*, pp. 63-68, April 2009
- C. Yang and A. Orailoglu, "A light-weight Cache-based Fault Detection and Checkpointing Scheme for MPSoCs Enabling Relaxed Execution Synchronization," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 11-20, October 2008
- C. Yang and A. Orailoglu, "Predictable Execution Adaptivity through Embedding Dynamic Reconfigurability into Static MPSoC Schedules," in *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, pp. 15-20, October 2007
- C. Yang and A. Orailoglu, "Light-weight Synchronization for Inter-processor Communication Acceleration on Embedded MPSoCs," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 150-154, October 2007
- C. Yang and A. Orailoglu, "Power-efficient Instruction Delivery through Trace Reuse," in *the 15th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 192 – 201, September 2006
- C. Yang and A. Orailoglu, "Power-efficient Branch Prediction through Early Identification of Branch Addresses," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 169-178, October 2006

### ***Work Paper***

- C. Yang and A. Orailoglu, "Accelerating Coupled Applications through Register Level Communication between Processing Elements," in *the 4th Workshop on Application Specific Processors (WASP)*, pp. 51 – 59, September 2005