Atieh Lotfi

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Education

Ph.D., Computer Science (Computer Engineering) San Diego, CA
Department of Computer Science and Engineering, UC San Diego (GPA: 3.87/4) *Dec.2018*
- Advisor: Professor Rajesh Gupta
- Thesis: Fault-susceptibility mitigation and efficient use of resources in programmable accelerators

M.Sc., Computer Engineering – Computer Architecture
School of Computer Science and Engineering, University of Tehran (GPA: 18.91/20) Tehran, Iran
- Advisors: Professor Saeed Safari, Professor Zain Navabi *Aug. 2012*
- Thesis: Efficient checkpointing techniques in multiprocessor architectures

B.Sc., Computer Engineering
School of Computer Science and Engineering, University of Tehran Tehran, Iran
- Advisors: Professor Saeed Safari, Professor Zain Navabi *June 2008*
- Project: Error resiliency of multimedia applications in the event of transient errors

Research and Work Experience

Senior GPU Architect NVIDIA *Jan 2019– Present*

GPU Architecture Intern NVIDIA *July 2017– Dec. 2017*
- GPU resiliency

Research Assistant UC San Diego *Sept. 2013–Dec 2018*
- Compiler-assisted hardware resource optimization for FPGA and GPU accelerators, Software level fault mitigation for GPU and FPGA accelerators, High-level synthesis, Approximate computing,

Research Assistant University of Tehran *Sept. 2009–Apr. 2013*
- Fault tolerant techniques for multicore architectures
- Distortion and complexity aware parameter tuning model for the H.264/AVC encoder
- Multi-level test package, Memory Testing, HDL-based Test Evaluation Tool Set

Publications

1. Jeng-Hau Lin*, Atieh Lotfi*, Vahideh Akhlaghi, Zhuowen Tu, Rajesh K. Gupta, "Accelerating Local Binary Pattern Networks with Software Programmable FPGAs", Design Automation and Test in Europe (DATE), 2019. (*Equal contributions)
2. Atieh Lotfi, Nirmal Saxena, Richard Bramley, Paul Racunas, Philip Shirvani, "Low Overhead Tag Error Mitigation for GPU Architectures," *IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, June 2018.
3. Atieh Lotfi, Rajesh K. Gupta, "ReHLS: Resource-aware Program Transformation Workflow for High-level Synthesis," *International conference on computer design* (*ICCD*), Nov. 2017.
4. "Celerity: An Open-Source RISC-V Tiered Accelerator Fabric," 29th ACM/IEEE Symposium on High-Performance Chips (*HOTCHIPS*), Aug. 2017.
5. Atieh Lotfi, Rajesh K. Gupta, "RxRE: Throughput Optimization for High-Level Synthesis using Resource-Aware Regularity Extraction,"(poster) *FPGA'17,* Feb. 2017.
6. Atieh Lotfi, Abbas Rahimi, Amir Yazdanbakhsh, Hadi Esmaeilzadeh, Rajesh K. Gupta, "GRATER: An Approximation Workflow for Exploiting Data-Level Parallelism in FPGA Acceleration," Design Automation and Test in Europe (*DATE),* 2016.
7. Atieh Lotfi, Abbas Rahimi, Luca Benini, Rajesh K. Gupta, "Aging-Aware Compilation for GP-GPUs," ACM Transactions on Architecture and Code Optimization (*TACO*), vol. 12, issue 2, 2015.

8. Atieh Lotfi, Abbas Rahimi, Hadi Esmaeilzadeh, Rajesh K. Gupta, "SqueezCL: Squeezing OpenCL Kernels for Approximate Computing on Contemporary GPUs," Approximate Computing Workshop, Oct. 2015.
9. Mehdi Semsarzadeh, Atieh Lotfi, Mahmoud Reza Hashemi, Shervin Shirmohammadi, "A fine-grain distortion and complexity aware parameter tuning model for the H.264/AVC encoder," Signal Processing: Image Communication, vol. 28, issue 5, pp. 441-457, 2013.
10. Atieh Lotfi, Arash Bayat, Saeed Safari, "Architectural Vulnerability Aware Checkpoint Placement in a Multicore Processor," *18th IEEE International On-Line Testing Symposium(IOLTS'12),* Spain, June 2012.
11. Atieh Lotfi, Saeed Safari, "A Genetic-based Optimal Checkpoint Placement Strategy for Multicore Processors," *The 16th CSI International Symposium on Computer Architecture and Digital Systems*, 2012.
12. Atieh Lotfi, Parisa Kabiri, Zainalabedin Navabi, "Configurable Architecture for Memory BIST," *In Proc. Of 8th East West Design and Test International Symposium (EWDTS'11),* Sep. 2011.

Book Contributions:

- "Digital System Test and Testable Design with HDLs", Z. Navabi, ISBN 978-1-4419-7547-8, Springer, January 2011, developed material and helped writing, Chapter 11 (Memory Testing).

Teaching Experience

Teaching Assistant CSE Department, UC San Diego, USA Jan. 2017 - March 2017
- *Advanced Microarchitectures - Accelerator for Machine Learning*

Teaching Assistant CSE Department, UC San Diego, USA Jan. 2015 - March 2015
- *Computer Architecture Course*

Lab Instructor ECE Department, University of Tehran, Iran Sep. 2010 - Oct. 2012 (5 semesters)
- *Digital Logic Design Laboratory*

Teaching Assistant ECE Department, Worcester Polytechnic Institute, USA June. 2012 - Sep 2012
- *Computer Architecture Course*

Teaching Assistant ECE Department, University of Tehran, Iran Sep. 2011 - Dec. 2011 (3 semesters)
- *Computer Architecture Course*

Technical Skills

Programming Languages: C/ C++, Python, CUDA, OpenCL
Hardware Description Languages: Verilog, VHDL
Technical Tools: Xilinx Vivado HLS, Altera SDK for OpenCL, Altera Quartus, ModelSim, Matlab
Compilers: LLVM Compiler Infrastructure
Computer Architecture Simulator and Emulators: Simplescalar, Multi2sim

Honors and Awards

- Travel grant for ICCD conference, 2017.
- Travel grant for CRA-Women Grad Cohort Workshop, 2015.
- Fellowship Award, UCSD Department of Computer Science and Engineering, 2013-2014.
- Ranked 3rd among MSc computer architecture students, 2012.
- Ranked 4th/16,000 in the Iranian nationwide graduate entrance exam in Computer Engineering, 2009.

Selected Graduate Coursework

- Advanced computer architecture
- Advanced compilers
- Parallel computation
- Design and analysis of algorithms
- Digital system testing and testable design
- Fault tolerant computing
- Hardware security for embedded systems
- Validation and prototyping of embedded systems
- Design of digital systems with HDLs
- Database Systems
- Machine learning
- Low-power VLSI design