Panel: Design Closure: Hope or Hype?

Chair: Kurt Keutzer, University of California, Berkeley, CA
Organizers: Vic Kulkarni, Frequency Technology, Inc., Santa Clara, CA
Gloria Nichols, Aristo Technology, Cupertino, CA
Andrew B. Kahng, University of California, Los Angeles, CA

Abstract

It’s been one year since Richard Goering told us that the EDA RTL-to-GDSII world was about to change. What have we learned? Who’s winning, and who’s not? This panel, consisting of the leading large and upcoming players in this space, will deliver concrete data to differentiate leading approaches to achieving design closure. Does the solution lie in raw speed and RTL optimization, with the synthesis-place-route back end just a commodity? Does the solution lie in new metrics for design convergence, and symmetric multiprocessing platforms for efficiency? Does the solution lie in a holistic, unified architecture of data model and tools? Or does the solution lie in extensions and unifications of existing production-proven logic, timing, and layout optimization technologies? A hard-hitting panel session will reveal the answers!

Panelist Statements

Raul Camposano
Synopsys, Inc., Mountain View, CA

Design closure is the main value proposition of the current new generation of implementation tools. In addition to timing closure, signal integrity and reliability are becoming equally important. The market requires the capability of designing “blocks” of the order of 1M equivalent gates in one pass taking a few hours, achieving closure. The basic new technology that enables this consists of synthesis combined with placement which truly understands delay (rather than weighted wire segments), and routing capable of handling constraints which implement signal integrity and reliability. Finally, these blocks plus IP are integrated on a System on a Chip using design planning technology. This includes (manual or automatic) floorplanning, budgeting and top level shape based routing. We are deploying significant innovations in all these fields.

Jacob Greidinger
AristoTechnology, Cupertino, CA

Block-based design has three advantages over flat: (1) it is scalable to handle arbitrarily large designs; (2) it greatly facilitates distributed collaborative design; and (3) it provides a modular, incremental approach to design closure. This latter advantage is the focus of today's panel. Block-based design imposes a process whereby incremental and hierarchical measurements on all important design parameters, e.g., timing, die size, power, and signal integrity, are made available at any point during the process. As a design progresses through a block-based process, increasingly accurate data becomes available for each of the blocks and for the top-level interconnect, and the design is incrementally updated and adjusted to account for this new information. Each block will progressively become better defined, or “harden”, at different rates, until all blocks are hard and the final layout is done. Early hardening of one block will drive new re-budgeting for parts that are not yet implemented. This type of modular, incremental process, which is not possible using a flat approach, is essential for achieving a timely design closure for very large designs.

Patrick Groeneveld
Magma Design Automation, Inc., Cupertino, CA

Magma’s tool - Blast Fusion - achieves timing closure early in the design flow. The key breakthrough is Magma’s gain-based synthesis technology (called FixedTiming) that sizes each gate exactly to the proper value, maintaining optimal timing throughout the design process. The gain-based delay model has proven to be an excellent substrate for an iteration-free transition from the logical to the physical domain. Another advantage of the model is that signal integrity issues can be incorporated early in the flow. We believe that ‘flat’ design of multimillion gate chips will continue to co-exist with the hierarchical design styles. It is often overlooked that the use of physical hierarchy (block-level design) significantly affects timing and chip area. Moreover, it requires expert user intervention with detailed knowledge about the layout implications of circuit structure. Implementing a layout as 'flat' as possible will always result in a chip with better timing, area and power and fewer iterations. With Blast Fusion, tool capacity limitations and timing convergence issues are not forcing the use of a physical hierarchy. Multimillion gate chips can be designed flat on conventional 32-bit computers.

Michael Jackson
Avant! Corporation, Fremont, CA

VDSM interconnect at sub 0.18 micron process technologies poses significant time-to-market challenges for designers of next generation System-on-Chips. These challenges result from surprises between actual and expected interconnect loading and coupling at different stages in the design process and manifest themselves as chips failing timing and having signal integrity problems. Three distinct approaches have emerged to address these challenges: (1) Physical-based approaches with embedded synthesis technologies; (2) Synthesis-based approaches with embedded physical technologies; and (3) Glue-based approaches that seek to add value between the front-end (synthesis) and the back-end (physical). The single most effective way to address interconnect challenges is by leveraging the physical-based approach outlined above. During the panel discussion, the presenter will discuss for the reasons and advantages of the physical-based approach.

Larry Pileggi
Monterey Design Systems, Inc., Sunnyvale, CA

Any hope of deep submicron (DSM) timing closure requires either that: (a) system designers become physical designers, or (b) there is once again a design flow for which netlist signoff is
viable. Given the widening design productivity gap due to the increasing complexity of DSM systems and the short time-to-market schedules, however, the only real hope of timing closure is that some form of netlist signoff becomes a reality. Clearly such timing sign-off requires physical information below the floorplanning level of detail, but for design efficacy it should be at the highest level of abstraction possible. Monterey Design is providing a solution that first provides for reliable netlist sign-off at an early phase of the flow, managed by front-end logic designers. The physical design implementation can then be completed through detailed routing by maintaining strong correlation with the earlier predictions that were based on the same algorithms.

Lou Scheffer  
_Cadence Design Systems, Inc., San Jose, CA_

Users would like to specify a given function to be implemented on a chip, and then generate a design that meets all of their requirements - most notably speed, power, cost, and reliability (including all DSM effects). When they must iterate to do this, or worse yet they iterate and don't converge, they have a “design closure” problem.

The first requirement is that the tool give them an accurate prediction of downstream effects. Ideally they type RTL and get size and speed predictions. This must span from RTL (since that's what the user will change) to at least global route (needed for accuracy). The user at this level does not want to deal with physical hierarchy – the tool should appear flat.

The second and more difficult design closure issue is when the tool alone gives inadequate results. In this case the user must fiddle with the RTL, the logical to physical mapping, the floorplan, or the global route. In this case a hierarchical system with the minimum possible hierarchy is best. It must be hierarchical since humans can't handle large flat problems, but should be no more hierarchical than necessary to solve the problem.

Finally we note that DSM effects such as signal and design integrity are best solved by construction at the chip level and by correction at the block level.

Martin Walker  
_Frequency Technology, Inc., Santa Clara, CA_