

Wenjing Rao

University of California, San Diego
Department of Computer Science and Engineering
La Jolla, CA 92093-0404

Tel: 858-822-5313 (lab) 858-729-3963 (cell)

Fax: 858-534-7029

E-mail: wrao@cs.ucsd.edu

Web: www.cs.ucsd.edu/~wrao

Research Interests:

Nanoelectronic systems, Fault tolerance, Digital test, Design for testability,
VLSI CAD, Embedded systems

Education:

Ph.D CSE department, UC San Diego. GPA: 3.87/4.0 (2001-present)

Thesis: "Towards Reliable Nanoelectronic Systems"

B.S. CS department, Peking University, China. GPA: 3.4/4.0 (1997-2001)

Thesis: "Design and Analysis of A Single-Input-Change Test Pattern Generator"

Awards:

UC San Diego CAL-IT² Fellowship (2001-2003)

Guanghua Scholarship in Peking University 1998 (only top 5% eligible)

Excellent Study Scholarship in Peking University 1998 (only top 5% eligible)

Teaching Experience:

Instructor: (2006) Summer Session II, University of California, San Diego.

Undergraduate course: *Mathematics for Algorithm and System Analysis* (CSE21),

Solely responsible for developing course material and teaching.

<http://www.cse.ucsd.edu/classes/su06/cse21/>

Teaching Assistant: (2007, 2006, 2005, 2003)

Components and Design Techniques for Digital Systems (CSE140)

Computer Architecture Lab (CSE141L)

Introduction to Computer Architecture (CSE141)

Theory of Computability (CSE105)

Industry Experience:

Internship (2004): Summer quarter, Mentor Graphics Corp, San Jose, CA, USA

Participating in logic synthesis optimization for an FPGA based RTL synthesis tool.

Internship (1999): TCL Electronics Corporation, Shenzhen, China

Providing front level application engineering support.

Research Experience:

Research Assistant (2001-present): Reliable System Synthesis Lab, UCSD

Reliable construction of nanoelectronic systems.

Digital test, design for testability, built-in self test, test time and volume reduction.

VLSI CAD, embedded system.

Research Study (2001): Computer Architecture Lab, Peking University

Test pattern generator design.

Publications:

Journal Papers

1. W. Rao, A. Orailoglu and R. Karri, "Towards Nanoelectronics Processor Architectures", *Journal of Electronic Testing: Theory and Applications (JETTA), Special Issue on Test, Defect Tolerance, and Reliability of Nanoscale Devices*, in press, 2007
2. W. Rao, A. Orailoglu and R. Karri, "Logic Mapping in Crossbar based Nano Architectures", *IEEE Design & Test of Computers, Special Section on Computer-Aided Design for Emerging Technologies*, submitted, 2007

Conference Papers

1. W. Rao, A. Orailoglu and R. Karri, "Logic Level Fault Tolerance Approaches Targeting Nanoelectronic PLAs", to appear in *IEEE Design, Automation, and Test in Europe (DATE)*, April 2007
2. W. Rao, A. Orailoglu and R. Karri, "Topology Aware Mapping of Logic Functions onto Nanowire-Based Crossbar Architectures", *IEEE/ACM Design Automation Conference (DAC)*, pages 723-726, July 2006
3. W. Rao, A. Orailoglu and R. Karri, "Fault Identification in Reconfigurable Carry Lookahead Adder Implementations Targeting Nanoelectronic Fabrics", *IEEE European Test Symposium (ETS)*, pages 63-68, May 2006
4. W. Rao, A. Orailoglu and R. Karri, "Nanofabric Topologies and Reconfiguration Algorithms to Support Dynamically Adaptive Fault Tolerance", *IEEE VLSI Test Symposium (VTS)*, pages 214-219, April 2006
5. W. Rao, A. Orailoglu and R. Karri, "Architecture-Level Fault Tolerant Computation in Nanoelectronic Processors", *IEEE International Conference on Computer Design (ICCD)*, pages 533-542, October 2005
6. W. Rao, A. Orailoglu and R. Karri, "Fault Tolerant Nanoelectronic Processor Architectures", *IEEE Asia South Pacific Design Automation Conference (ASPDAC)*, pages 311-316, January 2005
7. W. Rao, A. Orailoglu and G. Su, "Frugal Linear Network-Based Test Decompression for Drastic Test Cost Reductions", *IEEE International Conference on Computer Aided Design (ICCAD)*, pages 721-725, November 2004
8. W. Rao, A. Orailoglu and R. Karri, "Fault Tolerant Arithmetic with Applications in Nanotechnology based Systems", *IEEE International Test Conference (ITC)*, pages 472-478, October 2004
9. W. Rao, I. Bayraktaroglu and A. Orailoglu, "Test Application Time and Volume Compression through Seed Overlapping", *IEEE/ACM Design Automation Conference (DAC)*, pages 732-737, June 2003
10. W. Rao and A. Orailoglu, "Virtual Compression through Test Vector Stitching for Scan Based Designs", *IEEE Design, Automation, and Test in Europe (DATE)*, pages 104-109, March 2003

Workshop Papers

1. W. Rao, A. Orailoglu and R. Karri, "Topology Aware Mapping of Logic Functions onto Nanowire-based Crossbar Architectures", in the proceeding of the 2nd *IEEE International Workshop on Defect and Fault Tolerant Nanoscale Architectures (NANOARCH)*, June 2006
2. W. Rao, A. Orailoglu and R. Karri, "Defect and Fault Masking in Nanofabric through Redundancy Adaption", in the proceeding of the 7th *IEEE Latin-American Test Workshop (LATW)*, March 2006
3. W. Rao, A. Orailoglu and R. Karri, "Architecture-level Fault Tolerant Computation in Nanoelectronic Processors", in the proceeding of the 1st *IEEE International Workshop on Defect and Fault Tolerant Nanoscale Architectures (NANOARCH)*, May 2005
4. W. Rao, A. Orailoglu, T. Wei, K. Wu and R. Karri, "Fault Tolerant Nanoscale Architectures", in the proceeding of the 6th *IEEE Latin-American Test Workshop (LATW)*, March 2005