

Chengmo Yang

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Research Interests:

Execution adaptivity and reliability enhancement in multicore systems, power- and thermal-aware system design, efficient on-chip communication and synchronization schemes, compiler-directed optimizations of embedded processors

Ph.D. Thesis:

Fine-grained and Predictable Execution Adaptivity in Multicore Systems

Advisor: Alex Orailoglu, Computer Science and Engineering, UC San Diego

Education:

- **Ph.D.** Computer Engineering UC San Diego 2003-present GPA: 3.93/4.0
- **M.S.** Computer Science UC San Diego 2003-2005 GPA: 3.93/4.0
- **B.S.** Microelectronics Peking University, China 1999-2003 GPA: 3.79/4.0

Publications:

Conference Papers

- C. Yang, M. Chen, and A. Orailoglu, "Squashing Microcode Stores to Size in Embedded Systems while Delivering Rapid Microcode Accesses," in *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, pp. 249-256, October 2009. **(best paper nomination)**
- C. Yang and A. Orailoglu, "Processor Reliability Enhancement through Compiler-Directed Register File Peak Temperature Reduction," in *International Conference on Dependable Systems and Networks (DSN)*, pp. 468-477, June 2009.
- C. Yang and A. Orailoglu, "Towards No-cost Adaptive MPSoC Static Schedules through Exploitation of Logical-to-physical Core Mapping Latitude," in *IEEE Design, Automation and Test in Europe (DATE)*, pp. 63-68, April 2009
- C. Yang and A. Orailoglu, "A Light-weight Cache-based Fault Detection and Checkpointing Scheme for MPSoCs Enabling Relaxed Execution Synchronization," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 11-20, October 2008
- C. Yang and A. Orailoglu, "Predictable Execution Adaptivity through Embedding Dynamic Reconfigurability into Static MPSoC Schedules," in *International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS)*, pp. 15-20, October 2007
- C. Yang and A. Orailoglu, "Light-weight Synchronization for Inter-processor Communication Acceleration on Embedded MPSoCs," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 150-154, October 2007

- C. Yang and A. Orailoglu, "Power-efficient Branch Prediction through Early Identification of Branch Addresses," in *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 169-178, October 2006
- C. Yang and A. Orailoglu, "Power-efficient Instruction Delivery through Trace Reuse," in *the 15th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, pp. 192-201, September 2006

Journal Papers

- C. Yang and A. Orailoglu, "Full Fault Resilience and Relaxed Synchronization Requirements at the Cache-Memory Interface," to appear in *IEEE Trans. on Very Large Scale Integration Systems (TVLSI)*, 2010
- C. Yang, M. Chen, and A. Orailoglu, "Minimizing On-chip Code Storage in Microcoded IPs while Delivering High Decompression Speed" invited for submission to the special issue of *the Journal on Design Automation for Embedded Systems*, 2010
- C. Yang and A. Orailoglu, "Orderly Execution Reconfiguration in MPSoCs through the Generation of Adaptive MPSoC Static Schedules," submitted to *IEEE Trans. on Dependable and Secure Computing*, 2010

Workshop Paper

- C. Yang and A. Orailoglu, "Accelerating Coupled Applications through Register Level Communication between Processing Elements," in *the 4th Workshop on Application Specific Processors (WASP)*, pp. 51-59, September 2005

Research Experience:

Research Assistant (2004-present), at ART (Architecture, Reliability, Testing) group, UC San Diego
 Research on the development of multicore architectures with aggressive compiler-directed, run-time execution adaptivity support, in the face of increasing levels of device unreliability and execution unpredictability, including

- cost-effective temperature reduction and communication acceleration techniques to maximally mitigate sources of execution uncertainty;
 - cache-based fault detection techniques to precisely identify resource variations
 - adaptive static scheduling techniques to quickly and predictably reconfigure the execution
- Additionally, to enhance computation efficiency, I have developed several architectural-level optimization techniques, including LUT-free, high-performance code compression, power-efficient branch prediction and instruction delivery techniques

Research Study (2002-2003), at MPRC (Microprocessor Research & Development Center), Peking University, China

- Instruction-level simulation & verification for SoCs
- Logic synthesis & static timing analysis for SoCs

Teaching Experience:

Teaching Assistant at UC San Diego for

- CSE 240A: "Principles in Computer Architecture" (2004, 2008, and 2009)
- CSE 120: "Principles of Computer Operating Systems" (2007 and 2008)

- CSE 140: “Components and Design Techniques for Digital Systems” (2004, 2008 and 2009)
- CSE 140L: “Digital Systems Laboratory” (2008 and 2009)
- CSE 141: “Introduction to Computer Architecture” (2004 and 2005)

Industry Experience:

Engineer Intern (Summer 2008, Summer 2007), at Broadcom Corporation, San Diego, CA
 Developing a behavior-level cycle accurate simulation and testing environment based on RTL description of application-specific SoCs

Engineer Intern (Summer 2006), at Mindspeed Technologies, Newport Beach, CA
 Developing a cycle accurate configurable system-level simulator for an application-specific SoC for voice processing products

Honors and Awards:

- Best paper nomination in CODES-ISSS 2009
- Samsung Scholarship in Peking University, October 2002 (only top 3% eligible)
- Dongshi Scholarship in Peking University, October 2001 (only top 3% eligible)
- Guangcai Scholarship in Peking University, October 2000 (only top 3% eligible)

Review Participation:

Reviewer for

- IEEE Trans. on Very Large Scale Integration Systems (TVLSI)
- Intl Conf. on Hardware/Software Co-design and System Synthesis (CODES-ISSS)
- Intl Conf. on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
- Intl Conf. on Computer Design (ICCD)

Assisted program committee members in reviews of

ISCA, ICCAD, DATE, DSN, LCTES (*Languages, Compilers and Tools for Embedded Systems*), SASP (*Symposium on Application Specific Processors*), NANOARCH (*Symposium on Nanoscale Architectures*), VTS (*VLSI Test Symposium*), ETS (*European Test Symposium*)

References:

- Brad Calder, Director/Architect, bcalder@microsoft.com
 Microsoft Corporation, 1 Microsoft Way, #109, Redmond, WA 98052
- Chung-Kuan Cheng, Professor, ckcheng@ucsd.edu
 CSE Department, UCSD, 9500 Gilman Drive, La Jolla, CA 92093-0404
- Keith Marzullo, Department Chair and Professor, marzullo@cs.ucsd.edu
 CSE Department, UCSD, 9500 Gilman Drive, La Jolla, CA 92093-0404
- Alex Orailoglu, Professor, alex@cs.ucsd.edu
 CSE Department, UCSD, 9500 Gilman Drive, La Jolla, CA 92093-0404
- Peter Petrov, Assistant Professor, ppetrov@ece.umd.edu
 ECE Department, U Maryland, 1421 A.V. Williams Bldg, College Park, MD 20742