Alex Orailoğlu

Computer Science & Engineering, UC San Diego, La Jolla, CA 92093-0114
Tel: (858) 534-0914 Fax: (858) 534-7029 email: alex@cs.ucsd.edu

Research Areas: VLSI Test & Fault Tolerance, Embedded Processors & Systems

Education:
S.B. *cum laude* in Applied Mathematics, Harvard College, 1977.
M.S. in Computer Science, University of Illinois, Urbana, 1979.
Ph.D. in Computer Science, University of Illinois, Urbana, 1983.

Professional Experience:
Professor of CSE, UCSD (1998-present)
Associate Professor of CSE, UCSD (1994-1998)
Assistant Professor of CSE, UCSD (1987-1994)
Senior Member of Technical Staff, Gould Research (1983-1987)

Technical Meeting Founder:
WASP, Workshop on Application Specific Processors (2002)
HLDVT, High Level Design Validation & Test Workshop (1997)

Publication Awards:
Best Paper Award, "Reducing test application time through test data mutation encoding" (with S. Reda), DATE, 2002
Best Presentation Award, "A Methodology for Software-Based Testing of Processor Control Subsystems: The Branch Prediction Case", (with S. Almukhaizim and P. Petrov), ITSW, 2001
Naveena Nagi Award, "Boosting the Accuracy of Analog Test Coverage Computation through Statistical Tolerance Analysis", presented to co-author S. Ozev, VTS, 2002

Keynote Talks:
NEWCAS, Northeast Workshop on Circuit & Systems, Montreal, PQ, *Customizable Embedded Processor Architectures*, June 03
Euromicro Digital Systems Design Symposium, Antalya, TURKEY, *Customizable Embedded Processor Architectures*, Sept 03
WRTLT, Workshop on Register Transfer Level Test, Xian, CHINA, Nov 03

Ph.D. Alumni:
Ramesh Karri, Associate Professor, EE, Polytechnic University, NY
Graduation (Aug 93) Position: Assistant Professor, ECE, UMass, Amherst
Thesis Title: *Automated Synthesis of Fault-Tolerant VLSI Systems*
Ian G. Harris, Assistant Professor, Assistant Professor, ICS, UC Irvine
Graduation (Apr 97) Position: Assistant Professor, ECE, UMass, Amherst
Thesis Title: *Microarchitectural Synthesis for Self-Testable VLSI Designs*
J. Laurence Goodby, MTS, Selectrix
Graduation (Oct 97) Position: MTS, Hewlett-Packard, Inc.
Thesis Title: *Test Synthesis and Self-Test in High Performance VLSI Digital Signal Processing*
Yiorgos Makris, Assistant Professor, ECE, Yale University, Jan 01
Thesis Title: *Transparency-Based Hierarchical Testability Analysis and Test Generation for Register Transfer Level Designs*
İsmet Bayraktaroğlu, MTS, SUN Microsystems, Nov 01
Thesis Title: *Extending the Reach of Self-Test Approaches in VLSI*
Şule Özev, Assistant Professor, ECE, Duke University, Oct 02
Thesis Title: *High Level Test Approaches for Mixed-Signal Systems*

MS Alumni:

Mahsa Vahidi, Design Automation Group Leader, Conexant, Inc., Mar 95
Thesis Title: *A Framework for Synthesis of Self-Testable Designs*

Kyriakos Lakkas, Jun 01
Thesis Title: *VLSI Design for Application Specific Reconfigurable Caches*

Service Awards:

IEEE Computer Society, Elected Golden Core Member, Sept 01

IEEE Computer Society, Certificate of Appreciation, Oct 00
IEEE Computer Society, Certificate of Appreciation, Oct 01
IEEE Computer Society, Meritorious Service Award, Oct 01
IEEE Computer Society, Certificate of Appreciation, Apr 02
IEEE Computer Society, Meritorious Service Award, Oct 02
IEEE Computer Society, Certificate of Appreciation, Oct 02

Community Service:

IEEE Computer Society Test Technology Technical Council:
Vice Chair (02-Present)
Chair, Tutorial & Test Education Program (02-Present)
Chair, Technical Activities Committee (01-02)

IEEE Computer Society:
Technical Activities Board
Chair, Communities (03-Present)

Executive Committee Member,
IEEE Computer Society Test Technology Technical Council (01-Present)
Operations Committee Member,
IEEE Computer Society Test Technology Technical Council (99-Present)
Executive Committee Member,
IEEE Computer Society Technical Activities Board (03-Present)

Distinguished Lecturer:

Polytechnic University, New York, *Effective Self Test Approaches for State-of-the-Art VLSI Designs*, Apr 02.

Tutorials:

IBERCHIP, BRAZIL, *High Level Test Synthesis Methodologies*, Mar 00
GRIAO, Montreal, PQ, *High Level Test Synthesis Methodologies*, Apr 00

Organizing Committee:

Program Co-Chair, Joint Hardware Software Codesign & International System Synthesis Symposium (Sept 02-Present)
Vice Program Co-Chair, IEEE VLSI Test Symposium (Apr 03-Present)
Program Chair, Workshop on Application Specific Processors (Jun 02-Present)
Finance Chair, IEEE VLSI Test Symposium (Apr 02-Apr 03)
Publication Chair, IEEE VLSI Test Symposium (Apr 00-Apr 02)
North American Liaison, Latin American Test Workshop (Mar 00-Feb 02)
General Chair, Workshop on Application Specific Processors (Jun 02-Present)
Program Chair, Workshop on Application Specific Processors (Jun 02-Present)
General Chair, HLDVT (Nov 98-Nov 99)
Program Chair, HLDVT (Nov 97-Nov 98)
Finance Chair, HLDVT (Nov 96-Nov 97)

Topic Coordinator:

Chair, BIST&DFT, Design Automation & Test in Europe (Mar 01-Mar 03)
Co-Chair, BIST&DFT, Design Automation & Test in Europe (Mar 00-Mar 01)
Chair, Embedded Core Test, International Test Conference (Oct 98-Oct 01)
Topic Chair, European Test Symposium (May 03-Present)

Steering Committee:	WRTLT, Workshop on Register Transfer Level Test (01-Present) HLDVT, High Level Design Validation & Test Workshop (00-Present)
Editorial Board:	**Associate Editor**, IEEE Design & Test (01-Present) **Associate Editor**, Journal of Electronic Test: Theory & Applications (02-Present) **Associate Editor**, IEE Digital Systems & Design (03-Present) **Associate Editor**, Journal of Embedded Computing (03-Present)
Program Committee:	International Conference on Computer Aided Design, ICCAD (Nov 02-Present) International Test Conference, ITC (Oct 96-Oct 01) VLSI Test Symposium, VTS (Apr 97-Present) Design Automation & Test In Europe, DATE (Mar 98-Present) European Test Symposium, ETS (Jun 00-Present) International Conference on SuperComputing, ICS (Jun 02-Present) International Conference on Hardware/Software Codesign, CODES (May 02-Present) International System Synthesis Symposium, ISSS (Sept 02-Present) Asian Test Symposium, ATS (Nov 01-Present) Defect & Fault Tolerance Symposium, DFT (Nov 99-Present) Asian South Pacific Design Automation Conference, ASP/DAC (Jan 03-Present) International Conference on Computer Design, ICCD (Oct 93-Oct 95) International Test Synthesis Workshop, ITSW (May 95-Present) Testing Embedded Core Systems, TECS (Nov 97-Present) IEEE International Workshop on Infrastructure IP, IIP (Oct 02-Present) International Online Test Symposium, IOLTS (July 96-Present) Electronic Design, Test and Application, DELTA (Jan 01-Present) VHDL International User's Forum (Apr 93-Apr 94) Latin American Test Workshop, LATW (Mar 00-Present) Brazilian Symposium on Integrated Circuit Design, SBCCI (Sep 02-Present) Northeast Workshop on Circuit & Systems, NEWCAS (Dec 02-Present) International Symposium on High Performance Computing, ISHPC (Oct 02-Present) International Workshop on Innovative Architectures, IWIA (02-Present)
Invited Talks:	Invited presentations at major US, Japanese and European Universities and industry including Intel, National Semiconductor, Hitachi, STARC, Japan, Philips, the Netherlands, Nara Institute of Science and Technology, Japan, University of Montpellier, France, Dortmund University, Germany, Delft University, the Netherlands, and numerous others.
Referee:	Have provided referee services to National Science Foundation panels, University of California, MICRO Program, major journals including IEEE Transactions on Computer-Aided Design and IEEE Transactions on VLSI Systems, major conferences including Design Automation Conference, Fault-Tolerant Computing Symposium, International Symposium on Microarchitecture and major book publishing houses.

SPONSORED RESEARCH AND EQUIPMENT GRANTS (1994-2003)

- National Science Foundation. "Application-Specific Reconfigurable Microarchitectural Enhancements for Embedded Processors in High Performance Hardware/Software Codesign", Alex Orailoğlu, 9/00-8/04, $390,404.
- National Science Foundation. "Synthesis of Self-Recovering and Fault-Secure Microarchitectures", Alex Orailoğlu, 7/93-12/97, $113,500.
- Semiconductor Research Corporation. "Mismatch Analysis for High Speed, DSM System Blocks & Simulation Methodology", Alex Orailoğlu, 5/01-4/05, $161,000.
- Semiconductor Research Corporation. "Behavioral BIST Insertion", Alex Orailoğlu, 9/93-12/96, $130,000.
- National Semiconductor Corporation. "Behavioral BIST Insertion", Alex Orailoğlu, 9/96-8/00, $102,000.
- Hughes Aircraft Company. "Self-Testable VHDL-Based Chip Generators", Alex Orailoğlu, 9/94-8/99, $147,000.
- Intel Corporation. "Microprocessor Testability Analysis", Alex Orailoğlu, 11/96-10/99, $106,000.
- Intel Corporation Research Equipment Grant. "Microprocessor Testability Analysis" Alex Orailoğlu, 2/97-2/99, $58,000.
- Conexant, Inc. "Design-for-Test and Test Generation Tools for Large, Industrial Designs", Alex Orailoğlu, 8/00-9/01, $22,500.
- SUN Microsystems. "Hierarchical Test Approaches for Realistic Fault Models and Test Sets", Alex Orailoğlu, 8/00-9/01, $30,613.
- National Semiconductor Corporation. "Analog/Mixed-Signal Test Translation & Analysis", Alex Orailoğlu, 8/00-9/01, $30,000.
- Texas Instruments. "Design-for-Test and Test Generation Tools for Large, Industrial Designs", Alex Orailoğlu, 8/00-9/01, $30,000.
- Agilent Corporation. "Mixed-Signal System-on-a-chip Test", Alex Orailoğlu, 8/00-9/01, $40,000.
- Hewlett-Packard, Inc. "Analog/Mixed-Signal Test Synthesis" Alex Orailoğlu, 7/99-8/00, $35,000.
- LogicVision, Inc. "Digital Signal Processing Test Synthesis" Alex Orailoğlu, 7/97-8/98, $20,000.
- Conexant, Inc. "Digital Signal Processing Test Synthesis" Alex Orailoğlu, 7/99-8/00, $20,000.
- Rockwell, Inc. "High Level Test Synthesis" Alex Orailoğlu, 7/97-8/99, $50,000.
- University of California, Micro Program, "Test Synthesis ", Alex Orailoğlu, 8/00-8/01, $41,188

- University of California, Micro Program, "Self-Testable VHDL-Based Chip Generators", Alex Orailoğlu, 9/94-8/98, $160,000.
- California Space Institute. "Hardware/Software Codesign of Highly Reliable VLSI Systems", Alex Orailoğlu, 7/94-6/95, $14,000.
- Design Automation Conference. "Synthesis of Self-Testable ASICs", Alex Orailoğlu, 7/95-6/96, $12,000.
- NATO Fellowship. "Synthesis of Fault-Tolerant Designs", Alex Orailoğlu and Hans-Joachim Wunderlich, 5/96, $5,200.
- SUN Microsystems Research Equipment Grant. "Synthesis of Self-Testable VLSI Designs", Alex Orailoğlu, 6/94, $11,985.

UNIVERSITY SERVICE

- Chair, Graduate Admissions Committee, 88-89, 95-97
- Chair, Affirmative Action Committee, 94-95
- Chair, Budget Committee, 98-00
- Chair, Computer Engineering Committee, 98-00
- Doctoral Advisor, SRC Graduate Fellow, Laurence J. Goodby, 95-97
- Doctoral Advisor, IBM Graduate Fellow, Ian G. Harris, 94-97
- Doctoral Advisor, IBM Graduate Fellow, İsmet Bayraktaroğlu, 00-01
- Doctoral Advisor, IBM Graduate Fellow, Şule Özev, 00-02
- Doctoral Advisor, IBM Graduate Fellow, Peter Petrov, 00-01
- Doctoral Advisor, IBM Graduate Fellow, Özgür Sinanoğlu, 01-03
- Mentor, UC Chancellor's Postdoctoral Fellow, Dr. M. Alston, 92-93
- Faculty Recruiting Committee, 97
- Computer Engineering Committee, 89-present
- Space Committee, 94-97
- Graduate Committee, 89-97
- Ph.D. Student Advisor, 90-92
- M.S. Student Advisor, 89-90
- T.A. Assignment and Development Committee, 90-95
- Mentor, Visiting Faculty Member, Dr. B. Atlas, 91-92
- Mentor, Visiting Faculty Member, Dr. L. Carro, 01
- Mentor, Visiting Faculty Member, Dr. A. Benso, 03
- Graduate Admissions Committee, 88-93, 94-99, 02-present
- Undergraduate Committee, 87-88

JOURNAL ARTICLES

1. Şule Özev, İsmet Bayraktaroğlu and Alex Orailoğlu. "Seamless Test of Digital Components in Mixed-Signal Paths" *IEEE Design & Test*, In Press, 2004.

2. Erika Cota, Luigi Carro, Alex Orailoğlu and Marcelo Lubaszewski. "Achieving Global Test Optimization in Core-Based Systems" *Journal of Electronic Testing: Theory and Applications*, In Press, 2004.

3. Şule Özev and Alex Orailoğlu. "Automated System-Level Test Development for Mixed-Signal Circuits" *International Journal on Analog Integrated Circuits and Signal Processing*, In Press, 2003.

4. Yiorgos Makris, İsmet Bayraktaroğlu and Alex Orailoğlu. "Enhancing Reliability of RTL Controller-Datapath Circuits via Invariant-Base Concurrent Test" *IEEE Transactions on Reliability*, In Press, December 2003.

5. Özgür Sinanoğlu, İsmet Bayraktaroğlu and Alex Orailoğlu. "Reducing Average and Peak Test Power through Scan Chain Modification" *Journal of Electronic Testing: Theory and Applications*, Vol. 19, No. 4, August 2003, pp. 457-467.

6. Şule Özev and Alex Orailoğlu. "Statistical Tolerance Analysis for Assured Analog Test Coverage" *Journal of Electronic Testing: Theory and Applications*, Vol. 19, No. 2, April 2003, pp. 173-182.

7. İsmet Bayraktaroğlu and Alex Orailoğlu. "Concurrent Application of Compaction and Compression for Test Time and Data Volume Reduction in Scan Designs" *IEEE Transactions on Computers*, In Press, Vol. 52, November 2003.

8. Özgür Sinanoğlu and Alex Orailoğlu. "Compacting Test Buses for Deeply Embedded SOC Cores" *IEEE Design and Test of Computers*, Vol. 20, No. 4, July-August 2003, pp. 22-30.

9. Alex Orailoğlu and A. Veidenbaum. "Application-Specific Microprocessors", *IEEE Design & Test of Computers*, Vol. 20, No. 1, January-February 2003, pp. 6-7.

10. Peter Petrov and Alex Orailoğlu. "Application-Specific Instruction Memory Customizations for Power Efficient Embedded Processors" *IEEE Design & Test of Computers*, January 2003, pp. 18-25.

11. Şule Özev, Christian V. Olgaard and Alex Orailoğlu. "Multilevel Testability Analysis and Solutions for Integrated Bluetooth Transceivers" *IEEE Design & Test of Computers*, Vol. 19, No. 5, September-October 2002, pp. 82-91.

12. Özgür Sinanoğlu and Alex Orailoğlu. "Efficient Construction of Aliasing-Free Compaction Circuitry" *IEEE Micro*, September 2002, pp. 82-92.

13. İsmet Bayraktaroğlu and Alex Orailoğlu. "Rapid Fault Diagnosis through Cost-Effective Deterministic Partitioning in Scan-Based BIST" *IEEE Design & Test of Computers*, Vol. 19, No. 1, January-February 2002, pp. 42-53.

14. Peter Petrov and Alex Orailoğlu. "Performance and Power Effectiveness in Embedded Processors - Customizable Partitioned Caches" *IEEE Transactions on Computer-Aided Design*, Vol. 20, No. 11, November 2001, pp. 1309-1318.

15. İsmet Bayraktaroğlu and Alex Orailoğlu. "Concurrent Test for Digital Linear Systems" *IEEE Transactions on Computer-Aided Design*, Vol. 20, No. 9, September 2001, pp. 1132-1142.

16. Yiorgos Makris, Jamison Collins and Alex Orailoğlu. "Fast Hierarchical Test Path Construction for Circuits with DFT-Free Controller-Datapath Interface" *Journal of Electronic Testing: Theory and Applications*, Vol. 18, No. 1, 2001, pp. 29-42.

17. Şule Özev and Alex Orailoğlu. "System-Level Test Synthesis for Mixed-Signal SOC Designs" *IEEE Transactions on Circuits and Systems II: Analog And Digital Signal Processing*, Vol. 6, No. 48, June 2001, pp. 588-599.

18. Samuel N. Hamilton, Andre Hertwig and Alex Orailoğlu. "On-Line Test for Fault Secure Fault Isolation", *IEEE Transactions on VLSI Systems*, Vol. 8, No. 4, August 2000, pp. 446-452.

19. Laurence Goodby and Alex Orailoğlu. "Pseudorandom-Pattern Test Resistance in High-Performance DSP Datapaths", *IEEE Transactions on Circuits and Systems, Part II*, In Press.

20. Laurence Goodby and Alex Orailoğlu. "Redundancy and Testability in Digital Filter Datapaths" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 5, May 1999, pp. 631-644.

21. Samuel N. Hamilton and Alex Orailoğlu. "Efficient Self-Recovering ASIC Design" *IEEE Design & Test of Computers*, Vol. 15, No. 4, October/December 1998, pp. 25-35.

22. Yiorgos Makris and Alex Orailoğlu. "RTL Test Justification and Propagation Analysis for Modular Designs" *Journal of Electronic Testing: Theory and Applications*, Vol. 13, No. 2, October 1998, pp. 105-120.

23. Alex Orailoğlu and Ian G. Harris. "Microarchitectural Synthesis for Rapid BIST Testing" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 6, June 1997, pp. 573-586.

24. Alex Orailoğlu. "On-line Fault Resilience through Gracefully Degradable ASICs" *Journal of Electronic Testing: Theory & Applications*, Vol. 12, No. 1/2, February/April 1998, pp. 145-151.

25. Alex Orailoğlu and Ramesh Karri. "Time-constrained Scheduling during High-Level Synthesis of Fault-Secure VLSI Digital Signal Processing" *IEEE Transactions on Reliability*, Vol. 45, No. 3, September 1996, pp. 404-412.

26. Alex Orailoğlu and Ramesh Karri. "Automatic Synthesis of Self-Recovering VLSI Systems" *IEEE Transactions on Computers*, Vol. 45, No. 2, February 1996, pp. 131-142.

27. Alex Orailoğlu and Ramesh Karri. "Coactive Scheduling and Checkpoint Determination during High-Level Synthesis of Self-Recovering Microarchitectures", *IEEE Transactions on VLSI Systems*, pp. 304-311, September 1994.

28. Ramesh Karri, Karin Högstedt and Alex Orailoğlu. "Computer Aided Design of Fault-Tolerant VLSI Systems" *IEEE Design & Test of Computers*, Vol. 13, No. 3, pp. 88-96, Fall 1996.

29. Ian G. Harris and Alex Orailoğlu. "Module Selection in Microarchitectural Synthesis for Multiple Critical Constraint Satisfaction", *VLSI Design: An International Journal of Custom-Chip Design, Simulation, and Testing.* 1997, vol. 5, no. 2, pp. 167-182.

30. Alex Orailoğlu and Ramesh Karri. "Synthesis of Fault-Tolerant and Real-Time Microarchitectures", *Journal of Systems and Software*, Vol. 25, No. 1, pp. 73-84, April 1994.

31. Alex Orailoğlu and Ramesh Karri. "Defect Tolerant Layout Synthesis" *International Journal of Electronics*, Vol. 76, No. 6, pp. 1121-1133, June 1994.

32. Alex Orailoğlu and Ramesh Karri. "The 'RELIABLE' Microarchitecture Synthesis System" *Journal of Computer and Software Engineering.*

33. Amir Hekmatpour, Alex Orailoğlu, and Paul Chau. "VLSI Design Framework based on Object-Oriented Modeling and Model-Based Reasoning" *IEEE Expert*, Vol. 6, No. 2, pp. 56-70, April 1991.

34. Ramesh Karri and Alex Orailoğlu. "Standard seven segment display for Burmese Numerals" *IEEE Transactions on Consumer Electronics*, Vol. 36, No. 4, November 1990, pp. 959-961.

BOOK CHAPTER

1. Alex Orailoğlu. "On-line Fault Resilience through Gracefully Degradable ASICs" in *On-Line Testing for VLSI*, edited by M. Nicolaidis, Y. Zorian, and D.K. Pradhan, Kluwer Academic Publishers, 1998.

2. Yiorgos Makris, Jamison Collins and Alex Orailoğlu. "Fast Hierarchical Test Path Construction for DFT-Free Controller-Datapath Circuits" in *10th Anniversary Compendium of Papers from Asian Testing Symposium*, 2001.

REFEREED CONFERENCE PUBLICATIONS

1. Özgür Sinanoğlu and Alex Orailoğlu. "Efficient RT-level Fault Diagnosis Methodology" *Asian South Pasific Design Automation Conference*, In Press, Jan 2004.

2. Özgür Sinanoğlu and Alex Orailoğlu. "Partial Core Encryption for Performance-Efficient Test of SOCs" *Proceedings of the International Conference on Computer Aided Design*, In Press, November 2003.

3. Peter Petrov and Alex Orailoğlu. "Compiler-Based Register Name Adjustment for Low-Power Embedded Processors" *Proceedings of the International Conference on Computer Aided Design*, In Press, November 2003.

4. Barış Arslan and Alex Orailoğlu. "Extracting Precise Diagnosis of Bridging Faults from Stuck-at Fault Information" *Proceedings of the IEEE Asian Test Symposium*, In Press, November 2003.

5. Özgür Sinanoğlu and Alex Orailoğlu. "Test Data Manipulation Techniques for Energy Frugal, Rapid Scan Test" *Proceedings of the IEEE Asian Test Symposium*, In Press, November 2003.

6. Özgür Sinanoğlu and Alex Orailoğlu. "Aggressive Test Power Reduction through Test Stimuli Transformation" *Proceedings of the IEEE International Conference on Computer Design*, In Press, October 2003.

7. Peter Petrov and Alex Orailoğlu. "Virtual Page Tag Reduction for Low-Power TLBs" *Proceedings of the IEEE International Conference on Computer Design*, In Press, October 2003.

8. Özgür Sinanoğlu and Alex Orailoğlu. "Modeling Scan Chain Modifications for Scan-in Test Power Minimization" *Proceedings of the IEEE International Test Conference*, October 2003.

9. Özgür Sinanoğlu and Alex Orailoğlu. "Hierarchical Constraint Conscious RT-Level Test Generation" *Euromicro Symposium on Digital System Design (DSD)*, September 2003.

10. Peter Petrov and Alex Orailoğlu. "Low-Power Branch Target Buffer for Application-Specific Embedded Processors" *Euromicro Symposium on Digital System Design (DSD)*, September 2003.

11. Peter Petrov and Alex Orailoğlu. "Customizable Embedded Processor Architectures" *Euromicro Symposium on Digital System Design (DSD)*, **Invited Keynote Paper**, September 2003.

12. Wenjing Rao, İsmet Bayraktaroğlu and Alex Orailoğlu. "Test Application Time and Volume Compression through Seed Overlapping" *IEEE Design Automation Conference*, Anaheim, California, June 2003, pp. 732-737.

13. Özgür Sinanoğlu and Alex Orailoğlu. "Parity-Based Output Compaction for Core-Based SOCs" *Formal Proceedings of the IEEE European Test Workshop, pp. 15-20*, May 2003.

14. İsmet Bayraktaroğlu and Alex Orailoğlu. "Decompression Hardware Determination for Test Volume and Time Reduction through Unified Test Pattern Compaction and Compression " *Proceedings of the IEEE VLSI Test Symposium*, April 2003, pp. 113-118.

15. Peter Petrov and Alex Orailoğlu. "Power Efficiency through Application-Specific Instruction Memory Transformations" *Proceedings of IEEE Design, Automation and Test in Europe Conference*, March 2003, pp. 30-35.

16. Wenjing Rao and Alex Orailoğlu. "Virtual Compression through Test Vector Stitching for Scan Based Designs" *Proceedings of IEEE Design, Automation and Test in Europe Conference*, March 2003, pp. 104-109.

17. Yiorgos Makris and Alex Orailoğlu. "Test Requirement Analysis for Low Cost Hierarchical Test Path Construction" *Proceedings of the IEEE Asian Test Symposium*, November 2002, pp. 134-139.

18. Özgür Sinanoğlu and Alex Orailoğlu. "Fast and Energy-Frugal Deterministic Test Through Test Data Correlation Exploitation" *Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, November 2002, pp. 325-333.

19. Özgür Sinanoğlu and Alex Orailoğlu. "A Novel Scan Architecture for Power-Efficient, Rapid Test" *Proceedings of the International Conference on Computer Aided Design*, November 2002, pp. 299-303.

20. Özgür Sinanoğlu, İsmet Bayraktaroğlu and Alex Orailoğlu. "Scan Power Reduction through Test Data Transition Frequency Analysis" *Proceedings of the IEEE International Test Conference*, October 2002, pp. 844-850.

21. Peter Petrov and Alex Orailoğlu. "Low-Power Data Memory Communication for Application-Specific Embedded Processors" *Proceedings of International Symposium on System Synthesis*, October 2002, pp. 219-224.

22. Şule Özev and Alex Orailoğlu. "Cost-Effective Concurrent Test Hardware Design for Linear Analog Circuits" *Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers*, September 2002, pp. 258-264.

23. Barış Arslan and Alex Orailoğlu. "Fault Dictionary Size Reduction through Test Response Superposition" *Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers*, September 2002, pp. 480-485.

24. Şule Özev, Hosam Haggag and Alex Orailoğlu. "Automated Test Development and Test Time Reduction for RF Subsystems" *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. 1, May 2002, pp. 581-584.

25. Peter Petrov and Alex Orailoğlu. "Energy Frugal Tags in Reprogrammable I-Caches for Application-Specific Embedded Processors" *Proceedings of International Symposium on Hardware/Software Codesign*, May 2002, pp. 181-186.

26. Sherief Reda and Alex Orailoğlu. "Reducing Test Application Time through Test Data Mutation Encoding" *Proceedings of IEEE Design, Automation and Test in Europe Conference*, April 2002, pp. 387-393. **Best Paper Award**

27. Peter Petrov and Alex Orailoğlu. "Power Efficient Embedded Processor IP's through Application-Specific Tag Compression in Data Caches" *Proceedings of IEEE Design, Automation and Test in Europe Conference*, April 2002, pp. 1065-1071.

28. Özgür Sinanoğlu, İsmet Bayraktaroğlu and Alex Orailoğlu. "Test Power Reduction for Embedded Cores through Minimization of Scan Chain Transitions", *Proceedings of the IEEE VLSI Test Symposium*, April 2002, pp. 166-171.

29. Şule Özev and Alex Orailoğlu. "Boosting the Accuracy of Analog Test Coverage Computation through Statistical Tolerance Analysis" *Proceedings of the IEEE VLSI Test Symposium*, April 2002, pp. 213-219.

30. İsmet Bayraktaroğlu and Alex Orailoğlu. "Gate Level Fault Diagnosis in Scan-Based BIST" *Proceedings of the IEEE Design, Automation and Test in Europe Conference*, April 2002, pp. 376-381.

31. Sherief Reda, Rolf Drechsler and Alex Orailoğlu. "On the Relation Between SAT and BDDs for Equivalence Checking" *Proceedings of International Symposium on Quality Electronic Design*, March 2002, pp. 394-399.

32. Şule Özev and Alex Orailoğlu. "An Integrated Tool for Analog Test Generation and Fault Simulation" *Proceedings of International Symposium on Quality Electronic Design*, March 2002, pp. 267-272.

33. Özgür Sinanoğlu and Alex Orailoğlu. "Space and Time Compaction Schemes with Minimum Test Application Time" *Proceedings of the IEEE International Test Conference*, November 2001, pp. 521-529.

34. Şule Özev, Christian V. Olgaard and Alex Orailoğlu. "Testability Implications in Low-Cost Integrated Ratio Transceivers: A Bluetooth Case Study" *Proceedings of the IEEE International Test Conference*, November 2001, pp. 965-974.

35. Özgür Sinanoğlu and Alex Orailoğlu. "Compaction Schemes with Minimum Test Application Time" *Proceedings of the IEEE Asian Test Symposium*, November 2001, pp. 199-204.

36. Sobeeh Almukhaizim, Peter Petrov and Alex Orailoğlu. "Faults in Processor Control Subsystems: Testing Performance and Correctness Faults in the Data Prefetching Unit" *Proceedings of the IEEE Asian Test Symposium*, November 2001, pp. 319-324.

37. İsmet Bayraktaroğlu and Alex Orailoğlu. "Selecting a PRPG: Randomness, Primitiveness, or Sheer Luck?" *Proceedings of the IEEE Asian Test Symposium*, November 2001, pp. 373-378.

38. Peter Petrov and Alex Orailoğlu. "Data Cache Energy Minimization through Programmable Tag Size Matching to the Application" *Proceedings of International Symposium on System Synthesis*, September 2001, pp. 113-117.

39. Peter Petrov and Alex Orailoğlu. "Speeding Up Control-Dominated Application through Microarchitectural Customizations in Embedded Processors" *IEEE Design Automation Conference*, June 2001, pp. 512-517.

40. İsmet Bayraktaroğlu and Alex Orailoğlu. "Test Volume and Application Time Reduction through Scan Chain Concealment" *IEEE/ACM Design Automation Conference*, June 2001, pp. 151-155.

41. Sobeeh Almukhaizim, Peter Petrov and Alex Orailoğlu. "Low-Cost, Software-Based Self-Test Methodologies for Performance Faults in Processor Control Subsystems" *Proceedings of the Custom Integrated Circuits Conference*, May 2001, pp. 263-266.

42. Özgür Sinanoğlu and Alex Orailoğlu. "RT-Level Fault Simulation Based on Symbolic Propagation" *Proceedings of the IEEE VLSI Test Symposium*, April 2001, pp. 240-245.

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