

Test Selection Based on High Level Fault Simulation for Mixed-Signal Systems *

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Abstract

Mixed-signal design and test tools are failing to keep pace with the increasing necessity for design exploration at the early stages. We outline a methodology and test set to enable test selection at the early design stages by providing a high level fault simulator and associated block-level modeling and traversal capabilities. Experimental results show that the outlined methodology provides superior fault simulation speed-ups while helping to minimize the test time for a mixed-signal receiver system.

1 Introduction

For any electronic system, data needs to be collected, transmitted and received in analog format, whereas digital processing of data yields much better quality as digital circuits are more immune to noise and variations in the manufacturing process. Today most electronic systems include both analog and digital components. In addition, recent technological developments enable integration of many mixed-signal components on one chip, increasing the popularity of mixed-signal Systems-on-a-chip (SOC).

While providing efficient and high quality solutions, SOC's bring about many challenging test problems. Traditionally, mixed-signal circuits are tested on a block by block basis by providing I/O access to each basic block. As the size and number of basic blocks in a typical system increase, such a test approach results in unacceptably high test overhead in terms of area, performance and test time. New system level approaches may provide great reduction in test time and performance overhead by compacting the test set and eliminating unnecessary test points.

In order to enable such a test compaction, an analysis of the system is needed to select a minimal test set that provides the required fault and yield coverages. A given input may provide coverage in terms of various specified parameters. Application of this single input may test more than one parameter, thus reducing the number of tests to be conducted. Fault simulation approaches aim

at evaluating a given test input in terms of the probabilities of rejecting a functional and of accepting a non-functional chip.

While in the digital domain fault models and fault simulation tools have matured, fault simulation and modeling in the analog domain is still in the definition phase. Most mixed-signal fault simulation and analysis tools operate at the transistor level. Transistor level approaches provide detailed and accurate analysis of the system. However, at the system level, computational complexity of low level analysis is unacceptable. Most of the proposed hierarchical fault simulation approaches also rely on detailed circuit simulators for fault effect propagation. In order to analyze the complete system in acceptable time, the level of abstraction needs to be raised. At the transistor level, faults in the analog domain are categorized as catastrophic faults or parametric faults [1]. Catastrophic faults are open or short circuits between two circuit nodes and parametric faults are unacceptable deviations in circuit parameters. When the level of abstraction is increased, both classes of faults map onto deviations in circuit parameters, thus becoming parametric faults. Continuity of parameters introduces a fundamental challenge in the analog domain as one component or parameter contains infinitely many faults. Moreover, while activating a fault or propagating the effect of a fault, one needs to incorporate acceptable variations in other circuit parameters.

This research aims at a basic block level parametric fault simulation methodology to help in selecting a minimal set of test inputs while providing the desired coverage. The fault simulation methodology computes the fault and yield coverage of a particular test that is defined as an input signal and output measurement methodology, such as amplitude measurement or FFT. While high level fault activation and fault effect propagation keeps the computational complexity manageable, process variations are incorporated through a probabilistic coverage criterion. Faults in circuit parameters are probabilistically distributed over the entire space which eliminates the problem of infinite number of faults. In case input or output signals are corrupted by noise or spurious components, the impact on fault and yield coverages needs to be computed. Therefore, these unwanted signals are

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tracked during propagation in order to compute coverages correctly.

This paper starts with an overview of research activities in mixed-signal fault simulation. Section 3 explains the proposed methodology. Section 4 discusses fault activation, propagation, and coverage computation in detail. Experimental results are given in Section 5 on a receiver system. Conclusions are presented in Section 6.

2 Previous Work

Fault simulators compute fault coverage by injecting a fault from a pre-defined set of faults and conducting some sort of simulation of the circuit under test. Most parametric fault simulators use the method of parameter perturbation for fault injection. In [2], output signal sensitivity to circuit components is utilized to compute an interval of acceptable deviation in output signals and to determine whether a certain deviation in a given parameter results in unacceptable output signal. This methodology requires computation of circuit sensitivities and necessitates specification of the faulty value. In [3], it is proposed that large reductions in simulation time can be achieved if the results of good circuit simulations are used as starting points for Newton-Raphson iterations, as the difference of fault-free and faulty circuit is infinitesimal. In [4], the authors extend this idea by combining it with Householder’s matrix update formula [5] to reduce the simulation time further both for DC and AC simulations.

Neural networks are utilized for fault simulation in [6]. After a neural network is trained through circuit simulations, it can be used to observe the output signals and determine whether the circuit contains a fault. In [7], the authors partition the circuit into smaller modules and extract a behavioral description of the modules. Transistor level faults are simulated and corresponding behavioral level faults are extracted. Behavioral simulations are then utilized for fault effect propagation. System level requirements are propagated to the input/output points of each module in [8] to determine whether faults in the modules can be detected by observing the given system-level specifications. For propagation, an I/O look-up table obtained by circuit simulations is utilized. Similarly, [9] aims at determination of the effect of transistor level faults at module level through the use of circuit simulations.

The approach proposed in this paper aims at utilizing fault simulation to help in selecting a minimal set of tests for a large mixed-signal system. The fault simulation approach differs from the aforementioned approaches by the level of abstraction and in the use of library-based models for basic blocks in the system so as to avoid time consuming circuit simulations. Parameter tolerances are incorporated through a probabilistic approach. Faults used in this methodology are also of probabilistic and continuous nature as discussed in [10]. Smaller deviations in parameters are more likely to occur while they are also

harder to detect. While the proposed approach can be used in conjunction with previously proposed lower level approaches, it provides a methodology of propagating input signal and fault effects at a higher level.

3 Methodology

For each basic block in the system, the parameters of the block impose requirements on the output signals when the input is specified. If the output signal does not satisfy the requirements, at least one of the parameters out of the specified range. When the basic block is tested by itself, near 100% fault and yield coverage can be obtained. The loss in coverage results from noise and error in measurements and limitations in sensitivity and accuracy of the measurement device as well as the specified test. When the basic block is integrated into a system, variations in parameters of other blocks may degrade coverage substantially. Therefore, fault and yield coverages of specified tests need to be computed in order to evaluate tests and the testability of the system.

The proposed fault simulation methodology has three basic steps. First, the specified test input is propagated to the input of each basic block that needs to be tested. For each specified parameter, the requirement on the output signal of the corresponding basic block is extracted. The requirement is then propagated to the primary output through other functional blocks as illustrated for the third order input intercept, IIP_3 , of a mixer in Figure 1.

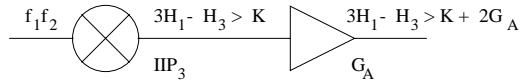


Figure 1: **Parameter Requirement and its Propagation**

Given the input signal in terms of frequency and power, the first order harmonic needs to exceed the third order harmonic by a certain amount at the output of the mixer, due to the IIP_3 requirement. When this requirement is propagated through the amplifier, the gain of the amplifier is used to compute the signal powers at the primary output, thus impacting the requirement. In this computation, the nominal value of the amplifier gain is used. However, the gain of the amplifier may vary within a certain tolerance. The variation in the amplifier gain may result in masking of some faults in the IIP_3 of the mixer. Analogously, some chips with acceptable IIP_3 may not satisfy the requirement at the primary output. In order to evaluate a given test input, the corresponding fault and yield coverages must be computed. This computation constitutes the last step of the fault simulation methodology.

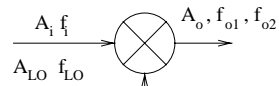
4 Fault Simulation & Test Evaluation

In order to extract the requirement imposed by a parameter, the primary input signal needs to be propagated to the input of each basic block. In the outlined scheme,

both the input signal propagation and the requirement propagation is enabled by a library-based approach. In this section, issues in modeling basic blocks and signals, requirement extraction and propagation, and test selection are discussed in detail.

4.1 Basic Block Library

The basic block library contains basic analog functional blocks, such as ADC's, mixers, and filters. Even though each class of modules may have various implementation styles, at the module level, its functionality can be expressed by simple input-output relations. The parameters of basic blocks play an important role in signal propagation as the output signal attributes depend on the basic block parameters as well as the input signal attributes. The values of these parameters are system specific and thus are supplied by the designer. In the analog domain, circuits exhibit some non-ideal behavior, such as spurious component generation or increased noise. Such non-ideal behavior is also expressed by some parameters, such as noise figure or third order input intercept point. These parameters have also been included in the basic block library in order to enable tracking of noise level and harmonic components in the signals. As an example, a simplified version of the mixer library model that we have constructed is shown in Figure 2.



Model: $A_o = G_M A_i$, $f_{o1} = f_i - f_{LO}$, $f_{o2} = f_i + f_{LO}$
Params: G_M
Non-ideal: BW, NF, Isolation, IIP_3 , P_{1dB}

Figure 2: Library Model of a Mixer

Basic block parameters that are used in signal propagation are specified as a nominal value with a certain tolerance. These parameters are distributed around the nominal value with a gaussian-like shape. In our scheme, this distribution is utilized in fault and yield coverage computations. If the standard deviation information is not available, the tolerance is assumed to be the 2σ point which corresponds to a 95% yield, a common yield value for typical mixed-signal basic blocks. Utilization of gaussian distributions provides an improved approximation of fault and yield coverages, as fault-free parameters are more likely to have small deviations. In addition, faults with smaller deviations are more likely to occur than faults with larger deviations, even though they are harder to detect.

4.2 Signal Components

In any mixed-signal system, signals are accompanied by unwanted components generated by environmental noise or system component non-idealities. Therefore, there exist fundamentally two kinds of signals propagating in a

mixed-signal path: desired and unwanted signals. An ideal signal can be accurately defined by its amplitude, frequency, phase and DC level in the time or frequency domain. These attributes can be computed from the given block parameters at any point in the system. However, unwanted signals such as noise are not as predictable. Whereas power spectral density of noise can be computed for a given system, phase and exact amplitude of noise is unpredictable. Similarly, clock spurs of a switched capacitor filter, or odd order intermodulation products of a mixer can be located in the frequency spectrum. However, their power or phase is hard to predict. Unwanted signals impose a second detectability criterion on faults in parameters. Desired signals must be above the noise level and must not coincide with harmonic components in the spectrum. This criterion is also used in fault and yield coverage computation.

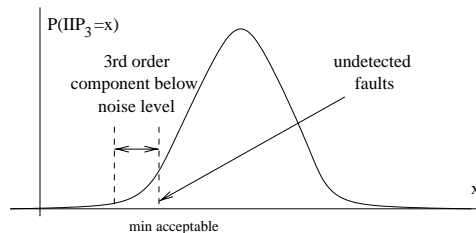


Figure 3: Undetected Faults due to Noise

As an example, consider the probability distribution of the IIP_3 requirement for a mixer as shown in Figure 3. If the input signal power is low, the third order component at the output of the mixer may fall below the noise level until the deviation in the IIP_3 of the mixer from the minimum acceptable value is sufficiently large. The faults between these two IIP_3 values are not detected. In a mixed-signal test evaluation scheme, in order to compute an accurate coverage, the noise level in the system needs to be tracked as well as other harmonic components. Prior to signal propagation, a noise analysis is conducted which computes the noise power levels at each point in the system using the input noise level and basic block parameters. Spurious components in the signal are computed during signal propagation.

4.3 Requirement Extraction

Each specified parameter imposes requirements on the output signal of the corresponding basic block. Depending on the input signal, or the measurement methodology, there may be several requirement types.

As an example, consider the cut-off frequency of the filter. If the specified input contains frequency components at the minimum and maximum acceptable cut-off frequencies, the gain at the minimum acceptable cut-off frequency must not be more than 3dB below the pass-band gain and the gain at the maximum acceptable cut-off frequency must not be less than 3dB below the pass-

band gain. However, if the input signal contains only one component around the expected cut-off frequency, the specified skirt slope needs to be used to compute the cut-off frequency. There are six different requirement extraction cases for the cut-off frequency parameter of any filter. These cases are summarized in Table 1. If the input signal does not satisfy any of the conditions in the table, no requirement is imposed on the output signal by the cut-off frequency parameter and the coverage of this test on cut-off frequency is nil.

Input contains	Requirement
$f_1 \in \{f_{pb}\}$ $f_2 = f_{cmin}, f_3 = f_{cmax}$	$G_1 - G_2 \leq 3dB$ $G_1 - G_2 \geq 3dB$
$f_1 \in \{f_{pb}\}$ $f_{cmin} < f_2 < f_{cmax}$	$G_1 - G_2 < \log(\frac{f_{cmin}}{f_2}) * S_{nom} + 3$ $G_1 - G_2 > \log(\frac{f_{cmax}}{f_2}) * S_{nom} + 3$
$f_1 \in \{f_{pb}\}$ $f_{cmin} < f_2 < f_3 < f_{cmax}$	$G_1 - G_2 < \log(\frac{f_2}{f_{cmin}}) * \frac{G_3 - G_2}{\log(f_3/f_2)}$ $G_1 - G_3 > \log(\frac{f_{cmin}}{f_2}) * \frac{G_3 - G_2}{\log(f_3/f_2)}$
$f_2 = f_{cmin}, f_3 = f_{cmax}$	$G_{pb} - G_2 \leq 3dB, G_{pb} - G_2 \geq 3dB$
$f_{cmin} < f_2 < f_{cmax}$	$G_{pb} - G_2 < \log(\frac{f_{cmin}}{f_2}) * S_{nom} + 3$ $G_{pb} - G_2 > \log(\frac{f_{cmax}}{f_2}) * S_{nom} + 3$
$f_{cmin} < f_2 < f_3 < f_{cmax}$	$G_{pb} - G_2 < \log(\frac{f_2}{f_{cmin}}) * \frac{G_3 - G_2}{\log(f_3/f_2)}$ $G_{pb} - G_3 > \log(\frac{f_{cmin}}{f_2}) * \frac{G_3 - G_2}{\log(f_3/f_2)}$

Table 1: f_c Requirements on the Output Signals

While extracting the requirement, if more than one input condition is satisfied, the case that leads to the least dependency on nominal parameters is selected. As an example, inputs satisfying the third condition shown in Table 1 are a subset of inputs satisfying the second condition. However, as the third case has no dependency on the specified skirt slope, it leads to improved coverage since faults are not masked by variations in the slope.

4.4 Requirement Propagation

The extracted requirement is propagated in a similar fashion to signal propagation. Given the input signals at each basic block, the corresponding output component is computed, and the requirement is modified accordingly. Since the variations in other parameters are used to compute the coverage, value substitution for parameters is delayed until the primary output is reached. At this point, the nominal values of parameters that are used in requirement propagation are substituted to compute the pass/fail criteria.

Propagation of the requirement imposed by the parameter under test is insufficient in determining final detection criteria and coverage. In order to detect the output signals and ensure that they are not corrupted by unwanted signals in the system, additional detection criteria

must be imposed at the primary output of the system. Unwanted signals basically consist of noise and harmonic response of basic blocks in the propagation path. Output noise level depends on the input noise level and noise generated by the basic blocks. If the input noise level is fixed for various test inputs, noise analysis needs to be conducted only once. Harmonic components in the output are due to the non-linear nature of analog components or switching effects. These components directly depend on the nature of the input signal and must be computed for all the specified tests. As additional requirements, the output signal levels need to be above the noise level and must not coincide with harmonic components in the frequency spectrum.

4.5 Fault & Yield Coverage Computation

If all the chips with acceptable parameters satisfy the requirements at the primary outputs, a perfect *yield coverage* of 100% is attained. Similarly, if all the chips that fail in one parameter fail to satisfy the requirements at the primary outputs, the *fault coverage* for tested parameters is deemed to be perfect. Frequently, the requirements involve other parameters as well as the ones under test. Since the exact values of these parameters are not known, their nominal values are used in the extraction and propagation of the requirements. The deviation in the parameters that are used in requirement computation causes misclassification. While such misclassification is unavoidable whenever tolerance and noise effects apply, we proceed to show an estimation method for identifying the extent of such misclassification in order to assist the designer in selecting the appropriate tests.

For fault and yield coverage computation, our goal is to compute the probability of misclassification of the given tests. For a specific parameter, p , a fault-free chip is rejected if the variations in other parameters result in the output requirement, r , not being satisfied. Therefore the probability of rejecting a chip with a fault-free p is:

$$\frac{P(p_{min} < p < p_{max})}{Y_p} \cdot (P(r < r_{min}) + P(r > r_{max}))$$

Similarly, the probability of accepting a faulty p is:

$$\frac{P(p_{min} > p) + P(p > p_{max})}{1 - Y_p} \cdot P(r_{min} < r < r_{max})$$

where Y_p is the yield of the parameter, p .

As an example, consider the mixer IIP_3 as in Figure 1. The requirement at the output of the mixer is:

$$3H_1 - H_3 > 2(IIP_{3min} + G_M)$$

When this requirement is propagated to the primary output, it becomes:

$$3H_1 - H_3 > 2(IIP_{3min} + G_M + G_A)$$

As a result, fault and yield coverages are given by the following relation, where $G = G_M + G_A$:

$$FC = 1 - \frac{\int_0^\infty P(IIP_3 = IIP_{3min} - x) P(G > G_{nom} + x) dx}{1 - Y_{IIP_3}}$$

$$YC = 1 - \frac{\int_0^\infty P(IIP_3 = IIP_{3min} + x) P(G < G_{nom} - x) dx}{Y_{IIP_3}}$$

In the above equations, the third harmonic is assumed to be above the noise level for simplicity. The distribution of the composite parameter, G , is computed out of the given distributions of G_M and G_A :

$$\mu_{(G_A+G_M)} = \mu_{G_A} + \mu_{G_M}$$

$$\sigma_{(G_A+G_M)} = \sigma_{G_A} + \sigma_{G_M}$$

4.6 Test Evaluation

The proposed scheme computes fault and yield coverage of a given set of tests for the targeted parameters in the system. Some tests may provide better coverage for a particular parameter but may result in poor coverage for another parameter. In order to provide a better evaluation, the fault and yield coverage results need to be composed for a given test. For two parameters that are tested with the same test input, coverages can be combined with the following relations:

$$p_1 \text{ and } p_2 \text{ requirements inversely correlated}$$

$$YC = 1 - (1 - YC_{p_1}) - (1 - YC_{p_2})$$

$$FC = 1 - (1 - FC_{p_1}) - (1 - FC_{p_2})$$

$$p_1 \text{ and } p_2 \text{ requirements not correlated}$$

$$YC = 1 - \frac{(1 - YC_{p_1}) + (1 - YC_{p_2})}{2}$$

$$FC = 1 - \frac{(1 - FC_{p_1}) + (1 - FC_{p_2})}{2}$$

$$p_1 \text{ and } p_2 \text{ requirements directly correlated}$$

$$YC = \min(YC_{p_1}, YC_{p_2})$$

$$FC = \max(FC_{p_1}, FC_{p_2})$$

The impact of a circuit parameter on the requirements of two other parameters defines the type of mutual correlation attribute of the impacted parameters. A worst case analysis needs to be followed in case of variant mutual correlation attributes for the same pair of parameters.

5 Experimental Results

The proposed fault simulation and test evaluation methodology is applied to a receiver channel architecture shown in Figure 4. The system is designed to have

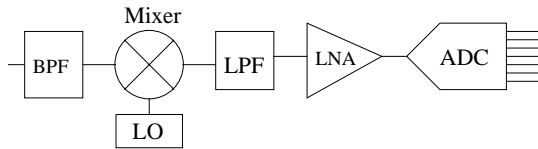


Figure 4: Experimental Set-Up

a signal to noise ratio of 15dB at the minimum sensitivity level of -70dB. The path gain starts from 48dB and can be increased to 54dB with 1dB gain steps which results in a dynamic range of 45dB. System parameters are

derived from a global transceiver specification set. The 10-bit ADC is allowed to have a 1LSB maximum differential non-linearity. Integral non-linearity must be less than 5LSB. For the experiment, three basic block level parameters are studied, IIP_3 of the mixer, f_c of the LPF, and DNL of the ADC. The specifications on these parameters are shown in Table 2.

Param	Req	σ	μ	tol
$IIP_3 >$	-22.5dBm	1dB	-20.5dBm	NA
f_c	500kHz	25kHz	500kHz	5%
$DNL <$	1.0LSB	0.2LSB	0.5LSB	NA

Table 2: Parameters Under Test

Fault simulations are conducted for four specified inputs; the output measurement methodology in each case is FFT. Three of the specified inputs are multi-tone sine waves whereas one is a pure sine wave. These inputs are shown in Table 3.

Power(dBm)	Frequency(MHz)	DC
-31	470.1, 470.2	0
-39	470.1, 470.45, 470.55	0
-31	470.1, 470.5	0
-28	470.1	0

Table 3: Specified Test Inputs

The first and the third tests are tuned for IIP_3 measurements. However, as seen in Table 4, one of these inputs has much better coverage for LPF f_c . For IIP_3 parameter coverage, the third order harmonic is a desired signal to be measured; it has basically no effect on f_c measurement, since the requirement for f_c is in terms of the gain difference between the two frequencies. However, this signal corrupts the spurious-free dynamic range, thus decreasing the coverage for DNL . Table 4 provides a complete summary of coverages.

Input	Parameter	FC	YC
-31dB 470.1MHz, 470.2MHz	IIP_3	96.1%	98.3%
	f_c	1.6%	100.0%
	DNL	0.8%	63.7%
-39dBm 470.1MHz, 470.45MHz, 470.55MHz	IIP_3	20.2%	96.3%
	f_c	99.8%	99.5%
	DNL	0.3%	34.2%
-31dB 470.1MHz, 470.5MHz	IIP_3	96.1%	98.3%
	f_c	93.9%	96.9%
	DNL	0.3%	63.2%
-28dBm 470.1MHz	IIP_3	0.0%	100.0%
	f_c	0.0%	100.0%
	DNL	25.0%	93.1%

Table 4: Fault Simulation Results

For multi-tone inputs, the requirement for IIP_3 is dependent on the mixer gain at the mixer output and is impacted by the gains of basic blocks in the propagation path. Fault coverage for IIP_3 is impacted by positive gain deviations, and yield coverage is impacted by negative gain deviations. For a single tone input, the IIP_3

Input	IIP_3, f_c, DNL		IIP_3, f_c	
	FC	YC	FC	YC
-31dBm, (470.1, 470.2)MHz	32.8%	87.3%	48.8%	99.1%
-39dBm, 470.1MHz, (470.45, 470.55)MHz	59.9%	76.7 %	59.5%	97.9%
-31dBm, 470.1MHz, 470.5MHz	64.43%	86.1 %	97.6 %	95.0%
-28dBm, 470.1MHz	8.3 %	97.7%	0.0%	100.0 %

Table 5: Combined Test Coverages

requirement cannot be extracted, so its fault coverage is zero. Output requirement of the f_c is dependent on the input frequencies. If the input is completely within pass-band, no requirement for f_c can be extracted, resulting in zero fault coverage. When two tones in the transition region are available, there is no need to include the skirt slope of the LPF in the requirement, resulting in higher fault and yield coverage. As the f_c requirement is not impacted by gains in the path, the requirements for f_c and IIP_3 are uncorrelated. The DNL parameter imposes spurious-free dynamic range requirements at the output. With multi-tone inputs, the mixer generates a high third-order harmonic, masking the faults in DNL , thus resulting in poor fault coverage for this parameter. For a single-tone input, spurious-free dynamic range is mainly determined by the ADC. High fault coverage for DNL can be achieved for the covered codes. The given sine wave of 100kHz at the input of the ADC covers 25% of the codes which sets an upper limit of 25% to DNL fault coverage.

Table 5 shows the composition of coverages for each of the tests. These coverage numbers together with the individual parametric coverage help in selecting the best tests in this case. For selection criteria, a minimal fault and yield coverage for each parameter needs to be satisfied. The input with the highest coverages is then selected. If a parameter coverage criterion is not satisfied, testability for that parameter is deemed unsatisfactory. It is observed that coverage on the DNL parameter is not satisfactory for any multi-tone signal. Moreover, the third test has the best coverage over IIP_3 and f_c parameters. As a result of this analysis, the third test is selected to cover both IIP_3 and f_c parameters. The ability to test both IIP_3 and f_c results in a substantial reduction of test time since testing of both parameters requires spectral analysis. However, for DNL , none of the tests yields acceptable coverage.

6 Conclusion

The inexorable push for higher levels of abstraction is all the more acute in the mixed-signal domain, as higher levels of integration result in increasing levels of analog/digital cohabitation on the same IC. The need to estimate a variety of design specifications, including area, performance and test time, necessitates novel approaches of high fidelity that are computationally effective and can

operate in an environment wherein all design information may not as of yet be available. As test costs consume even higher proportions of the design budget, it is all the more imperative that issues such as test time, fault and yield coverage, possible DFT locations, and number of test stimuli be estimated upfront. We introduce consequently in this paper a modeling capability and an associated high level fault simulation approach. We intend specifically to utilize such toolsets in test time reduction by rapidly identifying redundant tests that improve neither fault nor yield coverage. Such fault simulators are well suited to the task as the frequently overlapping nature of test coverage obviates the effects of possible inaccuracies in higher levels of modeling, prevalent any time abstraction levels are raised.

Specifically, we outline a test selection methodology based on a novel high level fault simulation approach. Input signal propagation, requirement extraction and propagation and computation of fault and yield coverages constitute the basic steps of the fault simulation approach. Desired signals are modeled by basic attributes of amplitude, frequency, DC level, and phase. Noise level and spurious components in the signals are also computed to achieve correct coverage computation. In order to enable signal propagation through functional blocks, a behavioral basic block library which captures both ideal and non-ideal parameters is implemented.

We apply the outlined methodology to an industrial-use mixed-signal receiver architecture. The outlined results indicate that substantial improvement in test time can be achieved when system level analysis is conducted.

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