Path-Based Test Composition for Mixed-Signal SOC's *

Sule Ozev and Alex Orailoglu
Computer Science and Engineering Department
University of California, San Diego
La Jolla, CA 92093
sozev@cs.ucsd.edu, alex@cs.ucsd.edu

Abstract

We outline a methodology for system level test composition out of module level tests in the context of SOC's. The method can be utilized as soon as high level specifications are available providing avenues for testability insertion. The digital/analog interface is handled by a conversion from digital bits to analog signals. Experimental results show that high fault and yield coverages for most tests can be attained with no hardware alterations.

1 Introduction

While digital test synthesis and associated DFT tools have a long history, manual approaches have been the norm in the analog domain to date. The main reason for this lag in analog test automation is that basic analog building blocks, such as filters, mixers, and DACs, have been traditionally fabricated as easily testable isolated elements. Yet recent developments in fabrication technology enable integration of mixed-signal systems composed of several functional blocks onto a single chip. Designers and test engineers have accumulated knowledge as to how individual functional blocks need to be tested so as to obtain adequate coverage. However, a system level composition of this test knowledge as a whole is lacking. Instead, costly DFT methods such as test point insertion are typically utilized in order to achieve direct test access to each functional block.

As the number of analog basic blocks in a system increases, the overhead of providing test access to each block in terms of I/O, area and performance becomes increasingly unpalatable. The highly limited number of analog sources and digitizers in mixed-signal testers poses an additional problem compared to the digital domain. The limitation in the number of analog ports necessitates frequent switching of analog sources and sinks of the tester. Settling times for analog source relays dominate data acquisition times and the overhead for initialization is nearly five times larger than test application times if the test input is switched each time. Even though frequent switching can be obviated by multiplexing all the test inputs and outputs to the same port, such approaches in turn result in increased complexity and performance overhead.

Test translation schemes fundamentally attempt to provide an answer to the problem of efficient test generation without resorting to costly and design-altering test additions. DFT overhead can greatly be reduced if existing functional signal paths in the system are utilized instead of explicit I/O access to the inputs and outputs of the modules. Such efficient and low-cost solutions can be attained by raising the level of abstraction. However, these benefits come at the expense fundamentally of some information loss that can result in reduced possibilities in setting appropriate controllability and observability characteristics.

Such controllability and observability concerns are not only prevalent but may possibly be of increased importance in the context of analog test translation. The situation is exacerbated as not only distinct values but also attributes with complex characteristics need to be modeled in order to ascertain correct primary input and expected primary output behavior. One such characteristic of analog circuits is parameter tolerances. Parameters of a defect-free circuit can vary within a range specified by the system designer. As a result, when only primary inputs are controlled and primary outputs are observed, it is not possible to determine the exact values of signal attributes at any point in the system. Such indeterminism in signals introduces a new and challenging controllability problem in the context of analog test translation.

Modeling basic blocks is another important step in signal propagation. Detailed models for basic blocks are often non-linear. In a test translation scheme, non-linear models are not desirable as they result in unacceptable computational complexity especially when backward justification is needed. However, sufficient information must be contained in basic block models in order to relate signals at the inputs and outputs. Moreover, in the test translation context, non-ideal responses of a basic block, such as noise and spurious response, must be included in the models to avoid degeneration of information.

In the analog domain, most tests are defined as a range rather than a single vector. In case the controllability and observability ranges do not overlap with a test range for a basic block, the test is not translatable to the system level. A portion of such untranslatable tests may be redundant for the system and therefore may be pruned away. The attributes of a test vector for a particular test must be set within a range

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where controllability and observability ranges overlap with the given test range for a viable test translation scheme. This requirement leads to a need of identifying system level constraints on a basic block's controllability and observability. The problem is further complicated by a variety of factors, such as parameter tolerances and noise, impacting controllability and observability at any point in the system.

In this paper, we outline a methodology for system level test synthesis for mixed-signal designs with a basic block level test translation approach. The proposed approach differs from the previous test generation approaches by the level of abstraction and in the use of library-based models for basic blocks in the system so as to avoid time consuming circuit simulations. The basic block library consists of most common building blocks of analog designs together with their ideal and non-ideal responses, such as noise figures and harmonic responses. Computational effectiveness is achieved through an early analysis of the system in order to identify feasible propagation paths. Parameter tolerances are incorporated through a probabilistic approach where the mean and the standard deviation of the parameters are used to compute probabilities of misclassification.

2 Previous Work

Although research in the mixed-signal test area has accelerated in the past 10 years, it still is far behind its digital counterpart. Several test generation approaches have aimed at finding the best test set for analog modules.

In [1], the goal is to select a subset of module parameters to measure and compute the rest of the parameters out of these measurements. The authors attempt to obtain a statistical relationship between the parameters to be measured and to be computed. Tests that do not have much effect on fault coverage are dropped out of the test set with a technique proposed in [2]. The authors aim at determining the specifications that are more likely to fail under the existence of parametric faults. When all faults are covered by measuring a set of specifications, there is no need to measure the remaining subset. Hence, test time is reduced.

In [3], the authors determine the cross correlation of an analog circuit, assuming that the circuit is placed between an ADC and a DAC. Since cross correlation is related to the impulse response of the analog circuit, a pass/fail condition can be determined on the basis of this value.

Automated generation of test stimuli is the aim of approaches outlined in [4, 5, 6], which employ output signal sensitivity, a concept introduced in [7], to circuit parameters. In [5, 6], test inputs are defined as single tone sinusoidal signals with frequency as an unknown parameter. The frequency at which the sensitivity of the output voltage (voltage gain) of the circuit is highest to a given component is selected to test it. Sensitivities are determined by manual analysis in [5] and by circuit simulations and the use of the adjoint network method in [6].

In the digital domain, problems with computational complexity of test generation for large systems and test justification have been encountered and several test translation methods have been proposed, such as [8, 9]. In [8], the goal is to identify transparent channels in the modules, through which tests for other modules can be propagated. In [9], the goal is to propagate pre-computed test stimuli and output responses of a module by utilizing only transparency and inverse modes of other modules. Not much hope can be drawn from a utilization of these methods in the analog domain as the concept of a single numeric value associated with a particular time point is not sufficient to capture all the relevant intricacies.

3 Methodology

Most tests for analog components are targeted at the measurement of certain block parameters and therefore are defined in terms of input signals and response measurement methods that satisfy certain conditions. Digital tests on the other hand are often defined as specific input vectors; the measurement method is always in terms of voltage. For both digital and analog components, the module level tests need to be synthesized at the system level. Non-functional digital test vectors are not targeted at parameter measurements; the only way to achieve system level test composition is to propagate the test vectors to primary inputs and outputs through other modules in the path. Analog or functional digital tests, on the other hand, can be translated to the system level either by propagating individual tests to primary inputs and output as in the digital case, or by designing a system level test targeted at the same path-level parameter as the original test. Since translation is performed on a test-by-test basis, it is worthwhile to conduct *a priori* an analysis of the system to determine which translation methodology and which test path will yield the best translation result. For example, if there are two paths to translate a particular test, the path that leads to the least information loss should be selected.

Due to variations in circuit parameters, it is impossible to achieve test translation of 100% accuracy. This inaccuracy results in some loss in fault and yield coverage. In order to evaluate the translated system level tests, fault and yield coverage of the targeted parameter need to be computed. In case of digital vectors, inaccuracy inhibits the translation of certain test vectors. These vectors need also be identified after pre-analysis is conducted.

3.1 Modeling

In a mixed-signal test synthesis system, signals must be modeled in an analog fashion to preserve test-related information and to enable propagation through analog modules. Theoretically, any signal can be defined as a combination of sinusoidal waves, with given amplitude, frequency and phase components. In practice, most analog tests are defined in terms of single or finite multi-tone sine waves, with each tone being treated as a separate signal. As a result, the proposed methodology models signals as sine waves, with tones propagated in parallel.

In addition, the DC level in signals is tracked in accordance with the dynamic component, as some blocks may be input biased and DC signals are utilized for digital vector propagation. Noise associated with analog signals can often corrupt the test information. If the level of corruption is not tolerable, translation is not useful. Therefore, the noise level in the system must be tracked in order to ensure correctness of test translation.

Basic block models should include necessary information to compute signal attributes while traversing through modules in the system. Simplicity for models is also important in a test translation scheme to keep the computational complexity manageable and to enable both forward and backward signal propagation. As a result, library models contain simple input relations, together with parameter tolerances, and expected non-ideal behavior. A more detailed explanation of the library models can be found in [10]. Digital modules can be modeled the same way as the analog modules, by setting parameter tolerances to zero. If a functional model of the digital block is not available, a digital bit cluster to analog signal attribute conversion needs to be conducted. This conversion leads to increased information loss; functional models are therefore utilized whenever they are available.

Parameter tolerances are incorporated into the model by a probabilistic approach. The parameters of a fault-free circuit have a gaussian-like distribution around a given nominal value. Therefore, the attributes of signals traversing through an analog circuit have a similar distribution. As an example, consider a typical amplifier gain distribution as shown in Figure 1. As this amplifier is traversed in a path, the signal amplitude at its output has a similar distribution around the nominal value which is computed from the input signal amplitude and the nominal gain of the amplifier. The standard deviation of the amplitude distribution can be computed using the standard deviations of the gain and the input amplitude. During pre-analysis, only the tolerance values associated with signal attributes are tracked in order to determine whether the resulting inaccuracy invalidates the translation of a particular test and to select the best translation path. During computation of system level tests, a more accurate estimation of the signal attribute distributions is computed in order to determine the probability of misclassification.

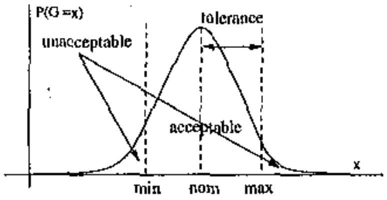


Figure 1. Typical distribution of an analog parameter

3.2 Digital/Analog Interface

During path traversal, the digital/analog boundary may need to be crossed in a mixed-signal system. In order to preserve signal integrity, one needs to reason about signals on each side of the boundary. Digital blocks that possess functional models can be treated the same way as analog modules. If such models are not available, a conversion from the signal attributes on the analog side to bit clusters on the digital side needs to be performed. This conversion is necessary even in the existence of functional digital models, if the digital test vectors are not functional. There are basically four different cases where the digital/analog boundary needs to be crossed:

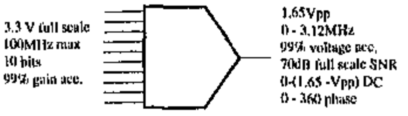


Figure 2. Digital/analog conversion for a 10-bit DAC

- **Propagating analog test inputs through digital cores:** When a cluster of digital bits is passed through a DAC, signal attributes at the output of the DAC can be computed out of digital parameters such as number of controllable bits, maximum and minimum clock frequencies, and gain tolerance of the DAC. Figure 2 shows a conversion for a 10 bit DAC, where all the input bits are controllable.

- **Propagating digital test input signals through analog cores:** The indeterminism in analog signals may prevent full controllability of digital bit clusters as the analog variations may be larger than 1 LSB of the DAC. The level of noise and inaccuracy in analog signals determines the number of digital bits that can not be controlled. The range of signal amplitude indicates the position of the fully controllable bit cluster and the frequency range determines maximum and minimum clock frequencies of the digital core.

- **Propagating digital test response through analog cores:** Signal conversion in this case is similar to analog input propagation. However, a 1LSB change in the corresponding analog signal can flip all the bits in the digital counterpart, thus resulting in misclassifications as shown in Figure 3. To avoid such misclassifications, the unobservable least significant bits must be set to the central value. For example, if the digital response of 1011xxxx needs to be propagated through the analog chain, setting the 4 LSBs to 1000 provides an error range of 3% for the analog counterpart of the circuit.

- **Propagating analog test response through digital cores:** This case is similar to propagating analog test inputs through digital cores. Analog signal attributes can be obtained from digital parameters.

3.3 Analysis

In order to determine the best test translation path, the noise level in the system, and the level of indeterminism associated with a path, a pre-analysis of the system is conducted. This analysis consists of traversing all possible

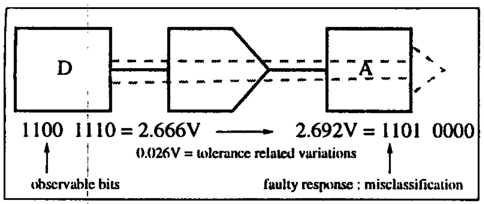


Figure 3. Misclassification due to analog variations

paths from primary input to primary output and vice versa to determine the ranges of signal attributes that can be propagated through modules, the noise level at each point in the system and the accuracy of signal attributes.

The analysis starts with the widest attribute ranges at the primary inputs (outputs). As basic blocks are traversed, the input-output relations are utilized to compute the ranges of signal attributes that can be obtained at the output (input) of each block. As an example, consider two blocks in a signal path as in Figure 4. At the input of Block A, signals that can be supplied by a tester are available. Frequency and amplitude ranges, accuracy, and noise are the same as the tester output. As Block A is traversed, its functionality limits frequency and amplitude ranges, decreases accuracy and increases the noise level; the resulting signal ranges are available at the input of Block B. Observable test responses are the ranges that the tester can measure at the output of Block B; however, the signals that can not propagate through Block B are not observable for Block A. Figure 4 shows amplitude and frequency ranges that can be propagated forward and backward for this path.

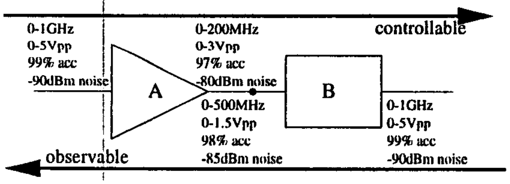


Figure 4. Signals that can be propagated in a path

3.4 Classification of Module Level Tests

In a test translation context, module level tests need to be classified into three categories at the system level so as to enable a reasoning on the methodology of test translation and a pruning away of untranslatable tests.

3.4.1 Untranslatable tests due to range deficiency

The range defined for a test may completely fall out of the amplitude and frequency operation ranges of all paths leading to primary inputs and outputs. Such tests are untranslatable to the system level through the use of existing signal paths. However, if these tests are within the operation of the targeted basic block, they may be redundant and substituted for by a system level test. An example of such redundant tests is the dynamic range test defined for a basic block. A certain block may have a wider dynamic range than the path it is serving in. However, testing for the path's dynamic range is adequate in terms of guaranteeing correct operation. In some cases, the test is out of the operation range of the targeted block and is of interest to the system. An example is the test for the cut-off frequency of a filter. If the test range defined for the cut-off frequency is not controllable or observable, the test is not translatable. However, there exists no easily identifiable system level test that can substitute for this particular test. Utilization of a DFT technique is unavoidable in such cases.

3.4.2 Untranslatable tests due to noise or inaccuracy

Inaccuracy in signal amplitudes, which is caused by tolerances of basic block gains, is the most frequently encountered problem in a test translation scheme that utilizes signal paths through analog modules. Tests that utilize the ratios of input and output signal amplitudes are targeted at measuring the gain of a basic block. Individual gains of basic blocks with errors within tolerance can not be determined independently of each other in a signal path. However, a composite variable, the path gain, can be measured with some error.

Measuring solely the path gain is insufficient in ensuring correct operation at the edges of the amplitude dynamic range of the signal path. A large positive gain deviation in a basic block may saturate the succeeding basic block at high signal amplitudes, but may be masked by gain variations of other basic blocks in the path when signal amplitude is low. Similarly, a large negative gain deviation in a basic block may cause the signal to disappear into the noise floor at low signal amplitudes, but may be masked by gain variations of other basic blocks in the path when the signal amplitude is high. Once the signal is corrupted by saturation or noise, it can not be recovered in the path. Two additional SNR tests at minimum and maximum signal amplitudes for the path detect such errors.

Dynamic range measurements require signals close to the noise level of a particular block. Since cascaded blocks add more noise on top, dynamic range measurement responses are most likely to be buried in the noise floor. Instead of testing the dynamic range of each block, the SNR of the path with minimum and maximum signal amplitudes might be measured. If the dynamic range of one block deviates from the nominal value such that it would change the system behavior, the SNR either at the maximum or at the minimum signal level will deviate from the desired value. Maximum and minimum operation signal amplitudes are determined from the given module parameters. Some test stimuli that result in output responses with small amplitudes can not be substituted by any system level stimuli. Offset error tests are typical examples. It is not possible to identify a composite test for the offset error measurements of individual blocks. Similarly, some non-functional tests may create small amplitude response that is buried in the noise level. Since non-functional vectors are not targeted at a specific parameter, these tests can not be translated. Such untranslatable tests must be identified so that a DFT methodology is applied to ensure high coverage.

3.4.3 Directly translatable tests

Among tests targeted for a basic block, a subset which satisfies the following conditions is directly translatable to system level:

- Frequency and amplitude of the desired stimulus and the output response fall into the available signal ranges for the basic block.
- The accuracy of computation is higher than the given threshold.
- Amplitudes of the stimulus and output response are higher than the noise level and within the dynamic range of the path.

If there are multiple paths that can be utilized for translation, the path that results in the highest test accuracy should be selected as the best path to conduct the translation.

3.5 Test Composition

Input signals and output responses of tests that are directly translatable are propagated through the signal path. If a digital module is encountered where the functional model is not available, D/A conversion is used as discussed in Section 3.2. The distributions of signal attributes are also computed along with the test inputs and outputs so that the probability of misclassification can be determined. A subgroup of tests that are not translatable through signal propagation can be combined with similar tests in a signal path and tested at the system level. In order to enable such a composition, the parameter that the tests are targeted at needs to be known. For example, the gain measurements in a signal path can be combined into a path gain measurement. This new test does not have high coverage in terms of individual parameters, but it has close to 100% coverage in terms of the path gain, which is a system level parameter. For tests that can not be translated to the system level with either approach, a DFT technique needs to be applied. A subset of bits in non-functional digital test vectors are propagatable through analog cores. Test point insertion is not necessary for such bit clusters. Test points then consist of bit clusters of a non-functional test vector that are not controllable or observable.

3.6 Evaluation

Raising the level of abstraction provides the necessary simplicity to handle large circuits. However this comes at the cost of some information loss. In order to quantitatively assess the level of information loss, fault and yield coverages of tests that are translated through signal propagation need to be computed. Misclassifications for analog parameters stem from the fact that a deviation in the parameter under test may be masked by deviations in other circuit parameters. Misclassifications in digital tests stem from the inability to set the unobservable least significant bits to the desired central value and variations in the analog circuit parameters. The probability, $\mathcal{P}_M$, of such misclassifications for testing a parameter, p, through measuring an output variable, v, can be expressed as:

$$\begin{aligned} & \mathcal{P}(p_{min} < p < p_{max}) \cdot (\mathcal{P}(v_{min} > v) + \mathcal{P}(v > v_{max})) \\ + \quad & (\mathcal{P}(p_{min} > p) + \mathcal{P}(p > p_{max})) \cdot \mathcal{P}(v_{min} < v < v_{max}) \end{aligned}$$

If the unobservable LSBs bits can be set to the central value, the probability of misclassification for a digital non-functional test vector is zero. If this is not the case, this probability is a function of the unobservable least significant bits, and is given by the following equation:

$$\mathcal{P}_M = \mathcal{P}(\Delta V > V_{LSB})$$

where ΔV is the deviation in the measured voltage due to analog parameter tolerances and V_{LSB} is the difference of the unobservable least significant bits from zero or from the maximum value, whichever is smaller.

If the standard deviations of the parameters are not available, the tolerances assigned to the parameters are assumed to be at 2σ points. This corresponds to a yield of 90%. In the context of SOC's, often previously designed modules are utilized and the expected distributions of parameters are known at the time of the system design. For the newly designed modules, the goal yield is usually higher than 95%. As a result, assuming a 90% yield for modules whose parameter distributions are not available often results in pessimistic fault and yield coverage values.

4 Experimental Results

The test composition approach is demonstrated on an upconversion signal as shown in Figure 5. A set of system parameters that needs to be tested is shown in Table 1.

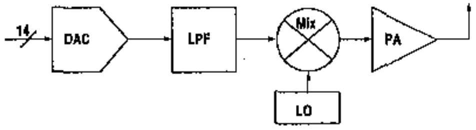


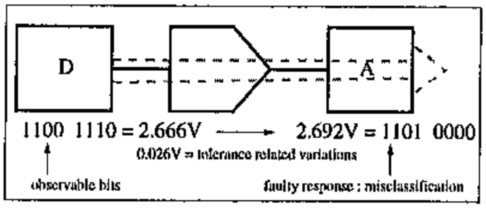
Figure 5. Experimental setup: Upconversion path

Additional parameters, such as the maximum clock frequency of the DAC, are utilized during pre-analysis or test translation to compute signal availability.

DAC	$DNL, V_{off}, INL, SFDR, G$
LPF	f_c, G, τ
Mix	G, IIP_3, NF
PA	G, IIP_3, NF

Table 1. Parameters to be tested

The ranges of signal attributes that can be propagated to the input of each block are shown in Table 2. The required tests are then compared with available signals at the inputs and outputs of each block and the test methodology is selected. Table 3 shows the system level tests corresponding to a variety of module level tests.



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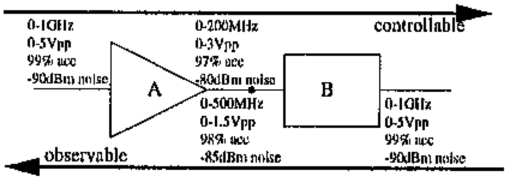

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