

Testability Implications in Low-cost Integrated Radio Transceivers: A Bluetooth Case Study*

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Abstract

As the use of wireless communications in daily life increases, attaining low-cost solutions becomes increasingly important due to shrinking profit margins. Cost optimization that solely targets at minimization of the cost of system architecture may result in sub-optimal, highly untestable, solutions. Test design and design for testability need to be incorporated into the system design flow to achieve viable solutions. This paper presents an analysis of test requirements, implications and test cost for low-cost Bluetooth systems. Testability problems are identified and possible solutions along with avenues to reduce the test cost by utilizing lower-cost testers are discussed.

1 Introduction

Wireless communications are becoming the norm for information transmission. Stringent market requirements and tight time-to-market windows call for low-cost solutions for radio-frequency subsystems.

Traditional design flows for a radio-frequency transceiver follow the path of system hardware cost minimization. Test design typically starts when the system design is nearing its end. However, decreasing profit margins and cost of chip production elevate test-related expenditures to an ever larger percentage of the overall manufacturing cost. The system with the lowest hardware cost may not be the lowest cost system, consequently, due to poor testability. In order to achieve optimal solutions, test design and test cost need to be incorporated into the overall design flow.

Bluetooth is an increasingly popular radio transceiver standard [1] that is designed to provide communication among a number of electronic components that are widely used in daily life, such as palm pilots, microwave ovens, etc. The intention of using Bluetooth systems on daily appliances imposes stringent requirements on manufacturing transceivers. Today, the target market value of a radio subsystem is \$2.50, with a 50% margin, implying a tolerable cost of a packaged and tested transceiver chip of \$1.25. Since

cost-effectiveness is the most important feature of the Bluetooth standard, its radio-frequency specifications are fairly relaxed when compared to other standards such as GSM or CDMA. Therefore, the importance of test cost is even more pronounced since the same set of specifications need to be tested regardless of how relaxed they might be.

In order to keep the test cost within acceptable bounds, system testability needs to be analyzed starting from early design stages. Testability problems need to be identified and addressed before the architecture and specifications are fully frozen. Design-for-testability changes need to be sought and incorporated to solve these problems. The cost of the tester equipment and test time also need to be incorporated into the analysis. The cost of a single second on a \$3M RF Tester comes to around a dime even if the tester is run constantly on a continuous, uninterrupted fashion. Alternative solutions utilizing lower-cost testers or even rack-and-stack equipment need to be considered to achieve a feasible overall design.

DFT solutions are not necessarily confined to the addition of hardware components, such as test busses and multiplexers, that would ease test application. The best DFT solution may be inherent in changing the underlying system architecture or adjusting the system specifications such that easy test application and lower tester cost are achieved.

In order to extract a set of performance parameters, a self-test strategy that utilizes sampled IQ modulation is presented in [2]. Most critical specifications, such as phase noise, blocker performance, and linearity cannot be tested with this strategy as it would require duplication of the complicated signal interactions and extraction of these parameters from the bit error rate (BER) that can be measured. In addition, BER requires long test times and is often quite difficult to measure correctly, as it is very sensitive to power level. Similarly, the authors discuss an overall approach to test the design of communication circuits with little emphasis on the measurement of radio-frequency specifications [3].

The goal of this paper is to demonstrate how testability analysis can be incorporated into the design flow at early stages so as to provide low-cost test solutions. Testability trade-offs of a radio system can be analyzed at multiple levels, such as architecture selection, parameter translation, and

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basic block implementation. In order to provide a case study, testability analysis on Bluetooth transceiver systems with no I/O access to internal blocks is presented in this paper. Tests are applied at the primary input and the responses are observed at the primary output. Testability problems are then identified and possible solutions to these problems are discussed. In the analysis we pursue, the goal is to identify tests that would require simple input stimuli and output response analysis. Approaches that utilize less costly test equipment are also discussed since state-of-the-art RF testers may be extremely expensive to utilize.

The next section discusses several possible transceiver architectures for Bluetooth compliance. Specifications of the receiver, transmitter, and synthesizer subsystems are derived in Section 3. Section 4 presents test requirements, testability problems and possible solutions. Hardware implications of designing an easily testable Bluetooth transceiver are discussed in Section 5. Conclusions are discussed in section 6.

2 Bluetooth Architecture Considerations

Test considerations need to be parallelized with design considerations for all the wireless systems. As the intended market niche of Bluetooth compliant systems requires low cost wireless solutions, the architecture must be optimized towards the lowest production cost. Such a requirement necessitates the use of minimal external components of smallest possible die area and lowest possible test cost. In order to achieve a viable solution, the chosen architecture must provide a maximum level of integration along with full incorporation of the particulars of the system.

The Time Division Duplex (TDD) property of Bluetooth enables decoupling of the transmit architecture from the receive architecture; they only need to share the frequency synthesizer. Such decoupling enables highly optimized architectures for the receive and transmit operations. Presently, the Bluetooth specification [1] includes a time limited relaxation of the receive specification¹ that can be utilized to further optimize the architecture. The following is a summary of possible architectures that have been used or considered for Bluetooth [4, 5] transceiver systems.

2.1 Receiver Architectures

Meeting the cost target of Bluetooth cannot be attained through external components for performing the channel selection in the receiver. Furthermore, the performance requirements of Bluetooth are so relaxed that a fully integrated solution should be feasible even without an absolute state of the art circuit performance. Naturally, one would like to beat

¹The specification relaxes in-band image frequencies and channels adjacent to the image frequency; these relaxations are typically geared towards low-IF receiver architectures.

the specifications with a reasonable margin, but it is unlikely that an improved sensitivity of a few dBs will justify a higher price point of a solution.

In general two types of direct conversion receivers are being utilized to achieve the desired level of integration. A zero-IF receiver down-converts the desired channel directly to base-band in IQ format (quadrature); a low-IF receiver down-converts the desired channel to a frequency close to base-band, and the signal is then filtered at this frequency, before the data is demodulated.

The true zero-IF receivers are from a filtering perspective the optimal solution, as simple low-pass filters at half the channel bandwidth perform the channel selectivity. Several problems with true zero-IF receivers make their design challenging. First, zero-IF receivers are quite sensitive to DC offsets which appear as part of the desired signal. Large DC offsets can easily saturate the complete receiver and result in high bit error rates (BER). The base-band processing can create the DC offset from offset within the blocks, but more importantly, it can be created by the down-converting mixer, where the LO signal can leak to the RF input, and cause a resulting DC offset. As this offset is created early in the receiver, its power will significantly increase throughout the receiver. Second, as the desired channel is converted directly to base-band, the flicker noise ($1/f$ noise) can pose a significant noise contribution that can degrade the sensitivity of the receiver. Last, if the LO leaks all the way to the antenna and gets reflected back by the surroundings, the DC offset is likely to be time varying as its phase will vary. An additional source of the DC offset is self-mixing of strong blocking signals. Therefore, the receiver must be able to remove the DC offset before demodulating the receive signal. A simple AC coupling of the receiver could potentially be used to remove the DC offset along with a portion of the desired signal. However, because of the TDD nature of Bluetooth, the settling of the bias levels may effect the receive operation; AC coupling is usually not utilized for zero-IF TDD systems, consequently.

Traditionally, the output quadrature signals are converted to the digital domain, and the demodulation is performed digitally. However, in the case of Bluetooth, the overriding importance of cost forces consideration of demodulator architectures where the down-converted signal is mixed back up to a lower IF frequency after filtering and the demodulation is performed using a simple limiter-discriminator demodulator.

Using a low-IF rather than the true zero-IF improves upon many of the drawbacks that the zero-IF receiver poses. As the desired signal is down-converted to an IF rather than at DC, self-mixing in the down-converting mixer will end up out of band and AC coupling can be used to remove the DC offset. Similarly, the flicker noise is not predominantly in-band. However, utilization of a low IF frequency requires significant image rejection as the mixer's image will reside

in-band. Several approaches can be used to address the rejection of the image. One could rely on an image rejection mixer solely, and then use a simple low-pass or band-pass filter. One can utilize an IF of half a channel that enables utilization of a low-pass filter to perform the channel selection. With the relaxed frequency accuracy of Bluetooth when including the worst-case scenario², a portion of the desired signal energy will spread across DC to the “negative” frequency domain. This may complicate the demodulation, and may also make it difficult to provide AC coupling in the receiver. Often a slightly higher IF, of one or two channels away, is utilized. For these receivers, complex filters are typically needed to introduce further image rejection as the blocker signal at the image frequency becomes stronger with increasing distance from the desired signal. Usually, the filter is implemented as a single-sided band-pass filter. Theoretically, sufficient image-rejection can be achieved with this implementation. However, mismatch may limit the obtainable image rejection. Furthermore, a complex filter requires double the amount of stages, thus increasing the die size and power consumption when compared to a simple low-pass filter required for a Zero-IF solution.

In the low-IF case, the receive signal can be demodulated with only one of the quadrature branches using a simple limiter-discriminator demodulator. As the other half of the complex filter is not utilized, its size can be optimized.³ If the signal is digitized directly at the chosen IF frequency, and the demodulation is performed in the digital domain, a higher power consumption of the ADC must be expected because of the higher sampling rate.

The low-IF receiver is a special case of a traditional super heterodyne receiver. One can also use a traditional super heterodyne receiver without introducing channel selectivity [5]. If a high-IF is used, the image moves out of band, so the front-end filter will attenuate the image. This requires a double conversion requiring two mixers and increasing the linearity requirements as well as the power consumption. In order to reduce the power consumption, a single VCO can be shared between the receive and the transmit chains [4]. In the case of the wide-IF receivers, the second mixer usually converts directly to base-band, thus obviating the issues of LO leakage to the antenna. An overview of some of the discussed architectures is presented in Figure 1.

2.2 Transmit Architectures

The TDD nature of Bluetooth ensures that the receiver and transmitter are not linked to each other. Still, in order to optimize die size, the frequency synthesizer should be shared between TX and RX. The transmit architecture must conse-

²The transmitter’s reference frequency being off in one direction, and the receiver’s off in the other.

³Both branches of the complex filter are required, but size optimization in the second branch may be possible. The integrated base-band channel select filter is usually the single biggest block on the RF transceiver.

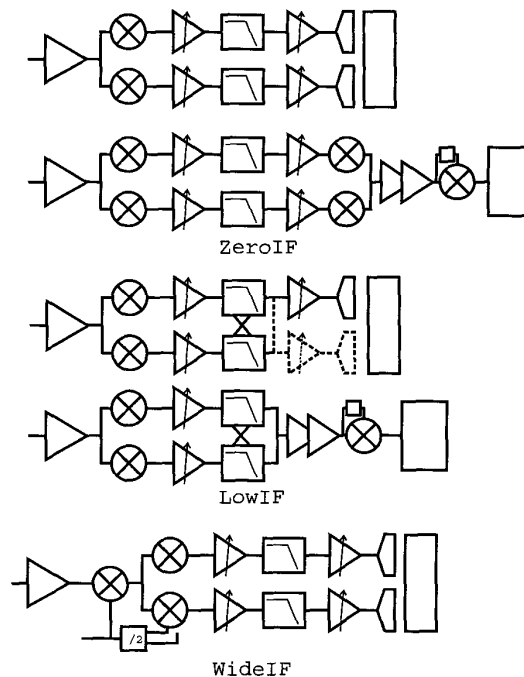


Figure 1. Possible Receive Architectures

quently be designed to use a synthesizer frequency in the range required for the receiver.

The traditional transmit architecture uses direct quadrature up-conversion of IQ signals. However, this architecture is really an overkill for Bluetooth, as the used Gaussian Frequency Shift Keying (GFSK) has no envelope information. GFSK can be implemented by modulating a VCO directly. Therefore, the two DACs and the multi-bit signal processing unit driving these DACs can be eliminated.

A typical approach to GFSK modulation is to open loop modulate the VCO [6]. Initially, the VCO is locked to the center of the desired transmit frequency. After the synthesizer loop is opened, the data is applied directly to the VCO through a gaussian filter. This low cost approach results in some significant problems both in terms of satisfying specifications and in terms of testability. If the transmitted signal power is high, the power amplifier is likely to push the VCO, drifting its frequency, when it ramps up. Furthermore, the loop must exhibit very low leakage to meet the frequency drift requirements in Bluetooth; the system is very sensitive to process variations.

A possible but slightly more complex solution is closed loop modulation of the VCO. Among the numerous existing approaches for closed loop modulation, Sigma-Delta modulation within the synthesizer is the most promising architecture. Even though this architecture results in a more robust solution in terms of process variations and frequency drift, the phase noise of the loop, both in-band and out-of-band,

still need to be measured. In addition, spurious components may appear due to component mismatch and non-linearity. As a result, transmit mask requirements may be more difficult to meet.⁴

Direct modulation of the VCO, both open-loop and closed-loop, severely complicates the ability to perform a true loop-back test of the system due to the modulation of the LO used to drive the receiver's downconversion mixer. Naturally, the system is not intended to operate simultaneously in transmit and receive mode. However, utilization of loop-back in test mode would enable performing all the tests at low frequencies, thus reducing the tester cost. Furthermore, loop-back test would enable built-in RF wafer sorting, which can significantly reduce the overall test cost.⁵ The use of a low-IF receive approach eliminates the possibility of loop-back testing as the transmit and the receive frequencies are at an offset from each other. The aforementioned transmit architectures are presented in Figure 2.

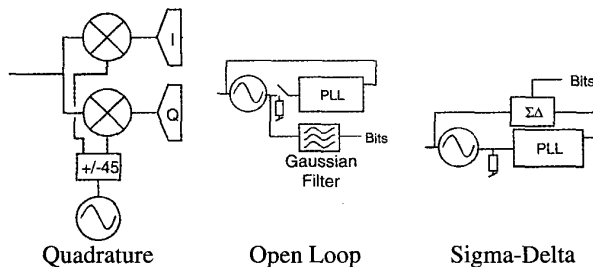


Figure 2. Possible Transmit Architectures

2.3 Synthesizer Architectures

The choice of the transmit architecture basically determines the synthesizer architecture. If the open loop approach is utilized in the transmit architecture, one can also consider its use during receive. This will reduce the noise produced by the PLL during receive if all noisy PLL logic is powered down when the loop is opened. However, since the receiver must be turned on for long periods of time to find the synchronization burst, the frequency drift is likely to become a problem.

2.4 Selected Transceiver Architectures

The goal of this paper is not the promotion of a particular transceiver architecture, but rather an examination of the testability of the different transceiver architectures; we restrict our attention to only relevant observations in this sense, generally. Yet an examination of testability considerations

⁴In this paper, it is assumed that the architecture supports the highest transmit power in Bluetooth.

⁵Eliminating most of the bad dies during wafer sort increases the yield of the final test, thus reducing the cost of rejected packaged dies as well as increasing the throughput of good dies.

at a lower level requires an elaboration on a concrete architecture; we focus consequently on receiver architectures that employ an ADC based digital demodulator in this context. This enables real measurement capabilities assuming that the raw data from the ADC converter can be processed. In the case of an analog demodulator, BER measurements are required, resulting in the need to employ complex test equipment that is capable of generating modulated receive signals.

In the following discussion, two different transmit and receive architectures are examined in regards to testability requirements. The two transmit architectures employ open loop modulation and sigma-delta modulation of a VCO, and the receiver architectures employ zero-IF and low-IF receive architectures.

The transmit test focuses on testing the transmit mask, the phase error, frequency drift, noise performance, and in-band spur levels.

On the receive side, a more block-based approach is considered, with focus on the filter characterization, VCO phase noise, PLL phase noise, and third order input intercept.

3 Bluetooth Specifications

Regardless of the underlying architecture, any Bluetooth system needs to satisfy certain minimum radio-frequency performance requirements. Even though the specifications relate to the full transceiver performance, it is possible to break them down to radio and radio sub-block performance requirements. In this section, we discuss the Bluetooth radio-frequency specifications and derive certain requirements both at the system level and at the basic block level. The complete set of specifications for a generic receive architecture is also extracted to enable testability analysis and discussion of possible design-for-testability solutions.

3.1 Receiver Specifications

The reference sensitivity for the Bluetooth system is specified to be better than -70dBm while the maximum signal level is -20dBm, resulting in a minimum dynamic range of 50dB.

Even though the effective bandwidth is lower than the specified signal bandwidth, a double-sided bandwidth of 1MHz is assumed for noise calculations. The thermal noise level at the primary input then will be -114dBm (-174dBm + 10log(1MHz)). The required noise figure can be determined from the required SNR at the input of the demodulator. Assuming that the demodulator requires a moderate SNR of 15dB in the presence of white noise, the noise figure of the path needs to be better than 29dB.

Channel sensitivity is defined by the blocking scenarios given in the radio-frequency specification [1]. The filter needs to suppress the given blocker to a level where a SNR of 15dB can be attained. At the 1MHz offset, the blocker

BT		Gain	N Fig	IIP3		Acc Gain	Ref Signal Level	Noise level
Component	[Typ.]	[Max. Act.]	IIP3	Effective	[Typ]	[Typ]	[Typ. Gain]	
1	Input	0	0	200	200	0	7.07E-05	4.46E-07
2	TX/RX Switch	-0.5	0.5	20	20	-0.5	6.68E-05	4.46E-07
3	Filter	-3	3	200	200	-3.5	4.46E-05	4.46E-07
Voltage Domain								
4	LNA	18	5.00E-07	0	0	14.5	3.54E-04	5.32E-06
5	RF mixer	6	5.00E-06	0	0	20.5	7.07E-04	1.46E-05
6	LP filter	-3	1.00E-05	200	200	17.5	5.01E-04	1.25E-05
7	Low-noise gain stage	16	1.00E-05	0	10	33.5	3.16E-03	1.01E-04
8	Channel Filter	12	5.00E-05	-20	40	45.5	1.26E-02	4.49E-04
9	Fine VGA	13	1.00E-04	0	60	58.5	5.62E-02	2.05E-03

Table 1. Bluetooth Receiver Specifications

has the same power as the desired signal; thus, it needs to be attenuated by 15dB. At 2MHz offset, the blocker is 30dB above the desired signal (at 10 dB above reference sensitivity), resulting in a 45dB required attenuation. The blocker at 3MHz is 40dB above the desired signal, which in this case is only 3dB above the reference sensitivity. Including the contribution from the thermal noise results in a required attenuation of 58dB, composed of 40dB of blocker power, 15dB of modem SNR, and 3dB of margin.

Linearity requirements are derived from the blocking specifications, where two strong (-39dBm) out-of-band signals which are spaced f and $2f$ respectively from the desired signal, result in an in-band interferer at frequency f by:

$$f_1 - 2f_2 = f_{desired} \pm 2f_{offset} - 2(f_{desired} \pm f_{offset}) = f_{desired}$$

The third order input intercept (IIP_3) requirement can be derived as follows:

$$IIP_3 > \frac{3P_{f_{1,2}} - (P_{ref} + 6dB - SNR - 2dB)}{2} = -20dBm$$

where $P_{f_{1,2}}$ is the power of the blocking signal and P_{ref} is the reference sensitivity level. It is assumed that an SNR of 13dB is adequate to meet the co-channel interference requirement. The 2dB is included to compensate for the contribution from thermal noise.

Even though the complete dynamic range of the receive chain is more than 50dB, the dynamic range requirements for the ADC can be much relaxed due to variable gain control of the amplifiers. The gain control algorithm needs to take into account issues such as fading margin and the thermal noise floor of the ADC. Assuming that the thermal noise floor of the ADC is at least 10dB below the accumulative noise and the required fading margin is 6dB, the desired dynamic range is 25dB, composed of 15dB of SNR, 4dB of quantization noise margin, and 6dB of margin. Therefore, a 5 bit ADC is adequate for meeting the minimum specifications. In practice, the dynamic range is often chosen slightly larger to ensure that ADC noise will not increase BER in case of strong signals. Still, the 30dB dynamic range offered by a 5 bit converter will suffice.

Generic Receiver Analysis: In order to enable a discussion of the testability problems and test solutions, a generic receive architecture as shown in Figure 3 is analyzed to derive a set of parameters. The set of resulting specifications for the receive chain analysis is given in Table 1.

3.2 Transmitter and Synthesizer Specifications

Most transmit side requirements are imposed on the synthesizer components, PLL and VCO, as the transmit circuit is basically composed of these two crucial elements. However, a set of system level specifications, such as RMS phase error, and transmit mask are given for the whole chain. The transmit power spectrum needs to be 20dB below carrier at the edge of the bandwidth. Out-of-band spectrum power is specified as -20dBm, 40dB below the transmit spectrum at 2MHz offset and at -40dBm, 60dB below the transmit spectrum at 3MHz.

Given a transmit architecture using VCO modulation, the VCO will be the dominant contributor to the noise in the adjacent channels. As the measurements are performed using 100kHz measurement bandwidth, an averaging will happen in the desired transmit spectrum, whereas the VCO noise power remains more or less constant in the portions of the spectrum further away from the carrier. If the transmit spectrum's 3dB bandwidth is assumed to be at 400kHz off the center, a correction factor of $10\log(800kHz/100kHz) = 9dB$ must be added. Moreover, a margin of 3-6dB is required to tolerate variations in the process. Therefore, the VCO specification for the transmit side becomes 60dB + 9dB + 4dB + $10\log(100kHz) = -123dBc/Hz$ at 3MHz. On the receive side, the blocker specification is used to derive the VCO phase noise requirements, as the blocker mixes with the VCO's phase noise and creates an in-band interferer. The

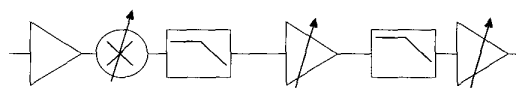


Figure 3. Generic Receive Architecture

phase noise requirement can be determined using the following equation:

$$\Phi_n(f) = P_{blocker} - P_{desired} - SNR - 3dB - 10\log(BW)$$

The 3dB is only required for the 3MHz blocker, but this poses the most stringent requirement. Combining the two phase noise requirements and a $1/f^2$ frequency roll-off for the VCO, the 1MHz reflection of the phase noise requirement becomes -114dBc/Hz. If frequency doubling is used, the actual VCO phase noise must be 6dB lower to compensate for the multiplication by 2.

RMS phase error specification imposes a limit on the synthesizer noise. In the closed loop modulation, this becomes the in-band PLL phase noise, and for the open loop modulation it becomes the integrated VCO noise. In order to achieve a symbol jitter better than 1/8 of a symbol time, the in-band noise floor needs to be around 85dB/Hz below the carrier.

Bluetooth also specifies levels of spurious emission. All spurs are required to be less than -40dBm, but 3 exceptions of up to -20dBm are allowed. These requirements once again are directly imposed on the synthesizer components, VCO and PLL, as requirements on VCO harmonics or PLL reference spurs.

4 Specification-Based Tests for Bluetooth

System specifications can be tested in many ways. Traditionally, basic blocks that make up a system are tested in an isolated fashion by providing external access to each basic block. Such an approach enables utilization of well-established methods at the basic block level. However, isolated block-based test not only is costly in terms of test time and hardware overhead, but also is unable to check for the interactions between the individual blocks. With the recently achieved levels of integration, block level testing is almost identical to full path testing due to the elimination of external components. One can also analyze all the possible failure scenarios at the system level and conduct a set of system level tests to check for these failures. Clearly, such an approach results in high test development time. In addition, applicability of the resultant test set is questionable since the testers, even with state of the art technology, are highly limited in signal generation and analysis when it comes to high frequency components.

An approach that combines the two extremes is to take advantage of the simplicity of block-based test and the convenience of system level application. Test signals and output analysis need to be as simple as possible, yet they need to guarantee system specifications. In order to achieve these goals, test design and analysis have to be an integral part of the system design flow. Testability requirements and the corresponding design implications have to be analyzed to enable trade-offs for the final architecture in terms of speci-

fications, on-chip test hardware and the complexity of the required tester.

In this section, we focus on the specifications of a general Bluetooth system most likely to induce testability problems and analyze the resultant test requirements. We assume that the test application is at the system level, i.e. that no access to the internal points in the system exists. Therefore, the results will be observed at the output of the ADCs. The goal is to use a single simple source to perform the testing, thus reducing the need for RF test equipment as much as possible.

4.1 Filtering Characteristics in the Receiver Path

The filtering characteristics on the receiver path are basically derived from the blocker and minimum SNR requirements. From the required attenuation levels, the filtering characteristics can be derived as shown in Figure 4.

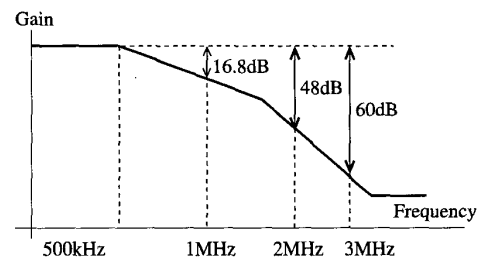


Figure 4. Required Filter Roll-off

The simplest way to test that the filter meets these requirements is to follow the points of the blocker specifications and apply a sinusoidal waveform to the system. The gains at these specific frequencies are then compared to the pass-band gain and a pass/fail decision is made on the attenuation. A multi-tone signal is both hard to generate at the desired frequency (2.5GHz), and hard to observe since the response at 2MHz and 3MHz is likely to be very small; if strong signals are used, intermodulation products are likely to be generated.

To get the best test results of the system, the full dynamic range of the ADC must be utilized. In the case of Zero-IF, one probably needs to reduce the signal power slightly to compensate for the DC component generated by self mixing in the receiver. It is assumed that even if the gain in the receiver is reduced, the noise figure will increase by less than the reduction in gain in order to ensure that the major contributor to the overall noise is the ADC. Therefore, the highest specified input signal power, -20dBm, should be used as it will guarantee the linearity of the receiver. When such a signal is applied, until the channel filter is reached, the minimum path gain will be in effect. Analyzing the automatic gain control and the block-level specifications of the example receiver, up to the channel filter, the gain is 17.5dB. However, since the blocker test signals will be suppressed by the channel filter, one can set the gain of the VGA following

the filter to a higher value for the out-of-band signals and still not saturate the ADC. Naturally, the gain of the VGA must be tested but as all measurements are relative to a desired signal in the pass band, this is easily achieved by inputting a fixed signal power and then setting the gain of the automatic gain controller (AGC). The only drawback of such an approach is the probability of saturating a component in the path. Luckily, the expected signal amplitudes can be computed and the gain can be adjusted to avoid saturation. Since the goal of this section is to discuss the measurement limitations, we assume that the maximum gain of the VGA does not saturate any of the basic blocks in the path. Such an adjustment results in a path gain of 46dB. Clearly, increasing the gain will also result in some increase in the thermal noise level. The resulting signal levels at the input of the ADC both for normal gain and for increased gain are given in Table 2.

Signal	ADC Input	
	Normal Operation Gain	Increased Gain
Desired	188.0mV	188.0mV
1MHz	43.1mV	188.0mV
2MHz	2.7mV	16.6mV
3MHz	0.7mV	4.3mV
Thermal Noise	1.7mV	3.5mV

Table 2. Blocker Test Signals Levels

The signal at 3MHz offset is near the thermal noise level. Therefore, this test needs to be shifted in frequency such that the output signal becomes appreciably stronger (at least 3dB) than the thermal noise. The attenuation at 3MHz can then be interpolated from the obtained data. Such an approach constrains the filter transfer function to have no zeros after the data point; the skirt slope is consequently not reduced. This is not a stringent constraint as the specified frequency is well outside the pass-band range.

Another test problem is that the signal at 2MHz is also weak. If a 5bit ADC is utilized, as suggested earlier, the signal will be below the quantization noise floor. Possible solutions to this problem and the cost-benefit trade-offs will be discussed in the next section.

4.2 Out-of-Band VCO Phase Noise

Both the receive path specifications and the transmit path specifications impose requirements on the VCO phase noise since it serves both paths. However, once the specification for the VCO is determined, it can either be tested in the receive path or the transmit path. As the goal is minimizing the number of high frequency tests, it is desirable to test the VCO phase noise in the receive path, as it will present the data at baseband allowing for inexpensive post-processing of the data.

As the receiver VCO phase noise requirements are derived from the blocking specifications, it is possible to perform the same test to measure the VCO phase noise. To mix

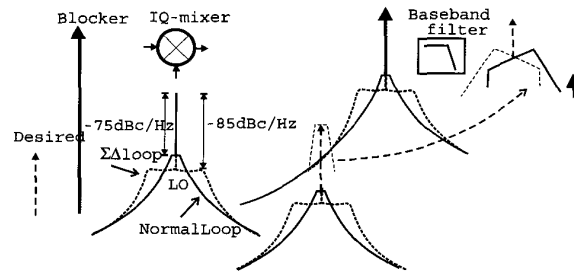


Figure 5. VCO and PLL Phase Noise Mixing

the out-of-band phase noise of the VCO into the bandwidth of the system, a sinusoidal signal at the desired offset needs to be applied. This waveform then will reflect the VCO's noise spectrum around the offset back into the band as shown in Figure 5. When the noise power, required to be 114dB/Hz below the carrier at 1MHz offset, is integrated over the band of interest, it becomes the test signal that needs to be observed. Since the fundamental will be suppressed by 16.8dB through the channel filter, one can set the gain of the VGA to its maximum (16dB typical), which results in a path gain of 43dB. The integrated VCO phase noise level will then be 6.3mV.

4.3 In-Band PLL Phase Noise

The major contributor to the in-band noise is the PLL phase noise. Once again, since a simple sinusoidal waveform at the input and spectral analysis at the output are required, it is advantageous to conduct this test through the receive path such that the output is at a lower frequency.

The in-band portion of the synthesizer noise is generated by the PLL and it needs to be -85dB below the carrier as shown in Figure 5. In order to emphasize the effect of the PLL phase noise, the fundamental signal needs to be at its maximum such that the resultant in-band phase noise is well above the thermal noise floor. If a sinusoidal input at the carrier frequency with the power level of -20dBm is applied, the path gain will be at its minimum (19dB), the integrated noise level at the input of the ADC at 11.2mV being the major contributor to the total noise level.

4.4 Third Order Intercept

Even though traditionally IIP_3 is tested on a per block basis, it is a system level specification and therefore can directly be tested as a pinout parameter.

Since IIP_3 basically specifies the linearity requirements of the system, its test requires a two tone signal. Two out-of-band sine waves with an in-band 3rd order harmonic are generally the best way to test for this parameter as the out-of-band attenuation can be utilized to suppress the fundamentals and allow the path gain to be increased. The power level of the two fundamentals needs to be 6dB below the full range to

avoid saturation which creates other frequency components that degenerates the desired harmonic.

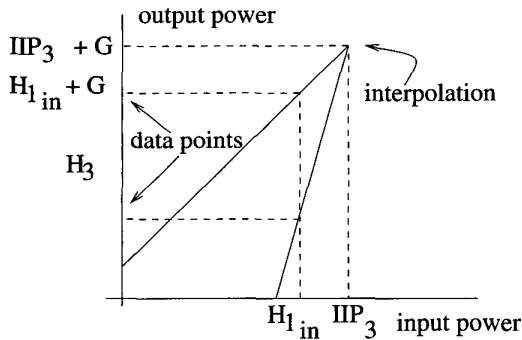


Figure 6. Interpolation of the IIP_3

As the IIP_3 parameter is a hypothetical point in the input range, it needs to be interpolated from the measured data as shown in Figure 6. Given the IIP_3 requirement and the input power, the harmonic power can be estimated by:

$$IIP_3 + G - H_3 = 3(IIP_3 - H_{1in})$$

$$H_3 = G + 3H_{1in} - 2IIP_3$$

The path gain until the channel filter is 1.5dB for the given signal amplitude. Assuming the two fundamentals are suppressed by the channel filter, the gain after this point will be 25dB. The IIP_3 parameter is specified to be above -20dBm. Plugging these numbers in, the test signal to be measured at the input of the ADC will be at:

$$H_3 = 26.5dB + 3(-26dBm) - 2(-20dBm) = -11.5dBm$$

Clearly, a better linearity than the specified value in the manufactured system implies a lower harmonic level. However, guaranteeing that one can observe this signal level at the ADC also guarantees full fault coverage on the IIP_3 parameter. The problem with this test is that it requires two signal generators, and usually additional filtering to remove the harmonics of the generators, that can easily dominate the measurements if not filtered.

The 1dB compression point parameter (P_{1dB}) is directly related to the IIP_3 parameter. Thus, one could consider measuring the P_{1dB} and computing the IIP_3 . Even though such a test requires only one RF source, it is likely to consume much longer test time due to the gradual gain roll-off and thus is rarely used.

4.5 RMS Phase Noise

The RMS phase noise directly affects the bit error rate of the system. There are basically two methods to test for RMS phase noise. Either this parameter is broken

down into more traditional parameters, such as DC offset, phase delay, and gain, or it is measured directly by utilizing modulation-demodulation and constellation of data-points. Whereas the traditional breakdown approach takes a longer test time, the direct measurement approach requires modulation-demodulation at the test equipment.

In either method, the lack of access to internal points in the system does not affect the test for RMS phase error, as it is a system level parameter tested at the antenna.

4.6 Transmit Mask

The transmitted signal has to satisfy a certain spectral mask in order not to pollute the frequency spectrum adjacent to the desired signal. The basic in-band contributors to the transmit power spectrum are the modulation power spectrum, PLL phase noise and the spurious emission. The VCO phase noise and spurious emission are the major out-of-band transmit power components. The resulting frequency spectrum is shown in Figure 7.

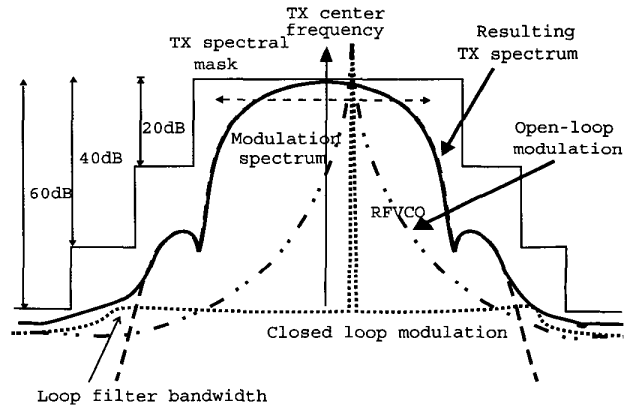


Figure 7. Contributors to the Transmit Spectrum

Attempting to check the complete transmit frequency spectrum using the receiver is not practical due to limited bandwidth, dynamic range, and number of samples. Furthermore, as the VCO is shared, the transmit mask can only be observed at one frequency. Thus, the transmit requirements must be tested by breaking down the spectrum contributors and testing specifically for them, unless expensive external test equipment is used. Among spectrum contributors, VCO phase noise is the major one; thus it needs to be tested. The test described above should suffice in this case.

The frequency spectrum of the GFSK modulation can easily be checked by down-converting the modulated carrier to a frequency where spectral analysis can be done. In-band spurious emissions need to be tested in a similar way, wherein the integration is not over the entire bandwidth, but rather by measuring power levels at specific frequencies. The basic

Spec	Input	Output	Measurement
Filtering	-20dBm Single-Tone	16mV (min)	Spectrum
VCO Phase Noise	-20dBm Single-Tone	6.3mV	Noise
PLL Phase Noise	-20dBm Single-Tone	11.2mV	Noise
IIP_3	-26dBm Two-Tone	71mV	Spectrum
RMS Phase Noise	Digital	Modulated Carrier	Down-conversion Demodulation Constellation
Spur Level	Digital	85mV	Spectrum
Frequency Error	-20dBm Single-Tone	188mV	Frequency
Frequency Drift	Digital	0dBm	Spectrum

Table 3. Summary of Test Requirements

requirement of such tests is the ability to down-convert the signal so that enough samples can be obtained to achieve adequate test accuracy. Even though such an approach requires external sampling equipment, it may be possible to use the receiver directly in the case of a zero-IF solution. If other architectures are chosen, one could consider driving the receiver mixer by an external source through a test port, and then using the receiver to perform the measurements. Utilization of the receiver can also be used to measure the transmit mask. However, such an approach requires sufficient isolation between the receiver and transmitter.

4.7 Frequency Accuracy and Drift

The absolute frequency of the VCO is allowed to vary within a certain tolerance. Further, it may drift in time with a limit of $400Hz/\mu s$ [1]. The frequency drift is particularly a problem with the open-loop transmit configuration. As the absolute frequency accuracy depends only on the used crystal, the issue becomes to test for the frequency drift.

In order to test for the absolute frequency accuracy, the receive path can be utilized by applying a fixed frequency signal. The loop is then opened, even though the normal mode is assumed to operate the synthesizer in closed loop during receive in order to cope with frequency drift during acquisition searches. The frequency drift can then be observed at the base band. Since there are no other components that would induce fluctuations into the frequency of the output signal, this test can easily be conducted in the integrated environment.

Table 3 shows a summary of the test requirements for the specifications that were considered.

5 Hardware Implications

Testability analysis and test considerations need to be parallelized with the system design in order to prevent costly iterations and last minute test point insertions into the system. For cost-effective solutions, one needs to analyze testability in terms of the test applicability, design considerations to enable test application, test equipment that needs to be used and test time.

5.1 Testability Problems and Possible Solutions

For the Bluetooth specifications, out-of-band VCO phase noise and filtering characteristics at 2MHz and above result in small signal amplitudes that are susceptible to fall below the quantization noise floor depending on the ADC resolution, as shown in Table 3. These results are obtained with respect to an example system designed to minimally meet the specifications. Even though such a system may be the most cost effective choice from a design perspective, the inherent testability problems increase the overall production cost. In this section, we discuss the possible solutions to change the system design so as to eliminate these testability problems.

In order to increase the observability of the test signals for the aforementioned two tests, either the power of the output signals or the resolution of the ADC needs to be increased.

Designing the system such that it can accommodate signal levels larger than the specified maximum and increasing the gain of the VGA after the channel filter in the test mode are the two possible solutions to increasing the output signal levels. Application of signals larger than -20dBm may result in compression at the mixer and high harmonic levels that may pollute the signal spectrum with the current mixer specifications. Therefore, increasing the maximum signal level means increased linearity specifications for the mixer, which results in more power consumption. Increasing the gain of the fine VGA in the test mode may be a lower cost solution.

An alternate solution consists of increasing the resolution of the ADC to reduce the quantization noise level. Clearly, such a modification has power and die size implications as well. The lowest-cost solution possibly lies in combining these possibilities, such that the power consumption and the die size are not appreciably increased.

Furthermore, it is advantageous to be able to decouple the receive LO and transmit LO. This decoupling will enable the use of an external source to drive the receiver, while the internal synthesizer is operated in the transmit section. Thus, the receiver can be used to test and measure the transmit signal.

Finally, it is advantageous to choose an architecture that will allow loop-back test at the die level, in order to detect defective parts during wafer sort.

5.2 Test Equipment and Test Time

The cost of test equipment and test time is also a major contributor to the overall manufacturing cost. While designing the system and the test plan, the underlying implications for the tester requirements also need to be analyzed. For example, an RF tester that costs about \$3M, effectively operating 20 hours/day, with a lifetime of 3 years, costs about \$0.11/sec. Several seconds on such an RF tester together with the overhead of loading the chip into the tester and settling times of the sources and switches can add up to a large percentage of the overall manufacturing cost.

Therefore, when designing the tests, one can look for alternate solutions, such as utilization of a lower cost tester or even rack-and-stack equipment. From Table 3, one can observe that there are two tests which require high frequency measurement: down-conversion and demodulation. Whereas these operations can easily be performed on an RF tester, alternate solutions lie in providing the down-conversion and demodulation on-chip, or on the test board.

Loop-back architectures allow for on-chip down-conversion/demodulation of the transmit signal. However, with an open-loop single VCO transmit architecture and low-IF receive architecture solutions, loop-back is not a possibility. In order to enable loop-back, power consumption has to be increased appreciably in the normal operating mode. Therefore, such a modification to the system is not cost-effective.

Providing down-conversion-demodulation on a test board is an alternate solution to utilizing an expensive tester. Since the transceiver chip does have the capability, the receive path of a known good part can be utilized for this purpose during production test. The utilized parts need to be characterized first as their parameters will effect the total measurement. For example, while measuring the RMS phase error of the transmit path, the RMS phase error of the utilized receive circuit needs to be incorporated. Such a characterization can even be done on the bench with no introduction of additional production test cost.

6 Conclusion

Radio-frequency test cost is becoming an increasingly large portion of the overall manufacturing cost. With low-profit margin systems, such as Bluetooth, the importance of test cost is even more exacerbated. The traditional flow of sequential system design followed by test design is not a viable solution to achieve optimal overall cost as the architecture solution that leads to the lowest chip production cost may at the same time lead to inordinate test costs. The optimal cost solution minimizes the overall manufacturing cost, including the test development cost, the cost of the required test equipment, and test time. This fact necessitates an analysis of system testability and incorporation of justifiable DFT so-

lutions, not only in terms of additional hardware, but also in terms of modifications to the underlying system architecture and specifications.

In this paper, we have illustrated that to achieve overall low-cost solutions testability should not be a design afterthought. Incorporating test considerations into early design stages can help in identifying testability problems at each level starting from architecture selection. Utilization of system requirements of Bluetooth transceiver systems to conduct a testability trade-off analysis is essential, as the cost-effectiveness of the overall Bluetooth solution is even more pronounced due to its application niche.

Even though the initial system contains no testability enhancements, such as test busses or test points, most specifications can be tested at the system level using the primary input and output by applying simple sinusoidal waveforms. The identified testability problems in terms of the low levels of several test responses can be easily solved through slight changes to the system specifications and architecture. Tester cost is also incorporated into the considerations. The analysis indicates that the use of low-cost test equipment can be enabled through utilization of a special test mode that enables the receiver LO to be decoupled from the transmitter, or through external down-conversion-demodulation on the test board.

This case study confirms that if testability considerations are integrated into the design flow of radio transceivers both at the architectural level and at the block level design, low-cost test solutions are both feasible and easy to achieve.

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