An Integrated Tool for Analog Test Generation and Fault Simulation[*]

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Abstract

High levels of design integration and increasing number of analog blocks within a system necessitate automated system-level analog test generation and fault simulation tools. We outline a methodology and toolset for specification-based automated test generation and fault simulation for analog circuits. Test generation is targeted at providing the highest coverage for each specified parameter. The flexibility of assigning analog test attributes is utilized for merging tests leading to test time reduction with no loss in test coverage. Further optimization in test time is obtained through fault simulations by selecting tests that provide adequate coverage in terms of several components and dropping the ones that do not provide additional coverage. The generated test set, fault and yield coverages in terms of each targeted parameter, and testability problems are reported by the tool.

1 Introduction

Traditionally, mixed-signal circuits are tested on a block by block basis by providing I/O access to each basic block. As the size and number of basic blocks in a typical system increase, such a test approach results in unacceptably high test overhead in terms of area, performance and test time. New system level approaches may provide great reduction in test time and performance overhead by compacting the test set and eliminating unnecessary test points.

To analyze the testability of the system in acceptable time, and to relate targeted parameters to measurable signal attributes, the level of abstraction needs to be raised. A viable solution to test generation and fault simulation also needs to take system level constraints into account and be applicable in early design stages so that testability problems can be identified and DFT solutions incorporated. Parameter tolerances play an important role in the measurement accuracy for the designed tests. The effect of such tolerances needs to be incorporated into the test generation methodology to ensure test quality.

In this paper, an integrated high level analog test generation and fault simulation tool is presented. Test generation aims at determining the attributes of test signals and measurement methodology for a given set of circuit specifications. System level constraints are determined through a library-based analysis utilizing operating range behavioral models, parameters, their tolerances and expected non-ideal behavior.

A single test input may provide coverage in terms of several specified parameters. Application of this single input may test more than one parameter, thus reducing the number of tests to be conducted. Fault simulation aims at evaluating a given test input in terms of the probability of rejecting a functional and the probability of accepting a non-functional chip. A test targeted for a certain specification is also evaluated in terms of the coverage it provides for other circuit specifications. By combining these coverage results and selecting the tests that provide the desired coverage levels for multiple specifications, the test set can be compacted and expensive tester time reduced.

While high level analysis keeps the computational complexity manageable, process variations are incorporated through a probabilistic coverage criterion. Faults in circuit parameters are probabilistically distributed over the entire space. The distinction between the faulty circuit and fault-free circuit is made based on specified thresholds on the parameter values. In this way, only one fault definition for each parameter exists, eliminating the problems of infinite number of faults.

The paper starts with an overview of research activities in the mixed-signal test domain. Section 3 presents the test generation and fault simulation methodology. Fundamental issues related to modeling, propagation and test evaluation are discussed in Section 4. Section 5 discusses fault simulation and computation of coverages. Experimental results on a receiver channel architecture are presented in Section 6 and conclusions discussed in Section 7.

2 Previous Work

While the analog test problem has been overlooked until not too long ago, a variety of test generation approaches have in recent years been proposed due to the increasing cost and importance of analog test.

Test time can be reduced by scheduling the test of the *most likely to fail* parameters first and discarding the tests that do not increase test coverage [1]. A number of approaches utilize the sensitivity of measurable parameters to circuit components and aim at determining the test input that maximizes

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this sensitivity [2, 3]. In [4], the targeted circuit is considered to be integrated between an ADC and a DAC enabling the use of digital patterns. In [5], the goal is to determine the slope and duration of input ramps that result in the highest distinction between faulty and fault-free circuits.

Most parametric fault simulators use the method of parameter perturbation for fault injection. In [6], output signal sensitivity to circuit components is utilized to compute an interval of acceptable deviation in output signals and to determine whether a certain deviation in a given parameter results in an unacceptable output signal.

3 Methodology

The goal of an analog test generation methodology is to find a set of test signal attributes that maximize the effect of a targeted specification on a measurable output signal. The deviations in the targeted specification can then be observed through the deviations in the output signal. The ideal test signal for a targeted specification not only maximizes the sensitivity of the output signal to that specification, but also minimizes the effects of other parameters on the output signal. Basic block specifications impose requirements on the output signals based on the input signals, circuit behavior, and a given tolerance. Therefore, for a particular specification, the input space can be partitioned in such a way so as to describe the requirement of that specification and how it is affected by other parameters.

These partitions basically define certain signal properties, such as its shape or the number of tones, and the ranges of its attributes, such as frequency and amplitude, for which the requirements hold. For most parameters, more than one partition can be defined for distinct input conditions. However, some portion of the input space is not covered by any of the partitions. For such input signals, the targeted parameter has no effect on the output signal; thus there is no need to consider such input signals for testing the parameter.

When the basic block is a stand-alone component, the ideal test input lies within the partition that has a minimal dependency on other circuit parameters. However, when the basic block is integrated into a system or a core, that particular test input may not be available as the system imposes controllability and observability constraints on the basic block. In addition, the parameter variations of other basic blocks in the system impact the accuracy of the measurement. In this case, the ideal test input lies within the partition that obeys controllability and observability constraints and displays minimal dependency on other system parameters.

The proposed tool utilizes a database of partitions, i.e. input signal attributes and corresponding requirements, for selection of test signals and determination of fault-free and faulty responses. The flow of the proposed tool is shown in Figure 1. First, system level constraints are determined through path traversal and the use of high level models. From the response database, partitions that obey these constraints are selected. The requirements of the selected partitions are propagated to the primary output. At this point, the fault coverage provided by each partition is computed utilizing the statistical distributions of the parameters that are involved in the final requirement. The partition that leads to highest accuracy is selected to test the targeted parameter. This partition may firmly define some of the signal attributes, and define ranges for some others, providing a level of flexibility in setting the test signal attributes. In order to allow test compaction, these attributes are not set until all tests are generated and overlaps between selected input partitions are determined. If tests of several distinct parameters result in an overlap in terms of input signal attributes, these attributes are set to the mid-point of the overlapping region, resulting in test compaction without compromising the fault coverage of any parameter.

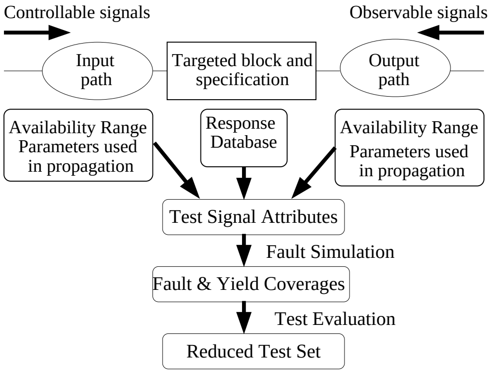

Figure 1. Flow of the tool

Generating the tests for each specification may result in large test set size and possible overtesting. Some of the generated tests may provide coverage in terms of several circuit parameters. Therefore, the test set can be compacted further by utilizing such tests and by dropping the ones that do not provide additional coverage. Fault simulation aims at evaluating a given test input in terms of the probability of rejecting a functional and the probability of accepting a non-functional chip.

In order to enable a second level of test compaction, each generated test input is then propagated through the system from the primary input to the primary output. For each specified parameter, the requirement on the output signal of the corresponding basic block is extracted. The requirement is then propagated to the primary output through other functional blocks. During this propagation, other circuit parameters may need to be utilized. The variations in these parameters cause a certain level of inaccuracy in the propagation which in turn results in misclassification of faulty and good circuits. Statistical distributions of circuit parameters are utilized to compute the level of such misclassifications in order to evaluate the given test set for several specifications.

4 Fundamental Concepts

Signal propagation approaches and the high level library are the two essential components of the proposed tool. In this section, issues related to signal propagation, and basic block, signal and test response modeling are discussed.

4.1 Determination of System Level Constraints

In the analog domain the input space is continuous, has multiple attributes and can take on an infinite range. The output space of a basic block on the other hand is limited by the operating range and parameters, where certain relations between input and output signal attributes hold. When several basic blocks are integrated into a signal path, the attributes of the signals that can be propagated through this path are limited by the behavior and operating ranges of all the basic blocks in the path.

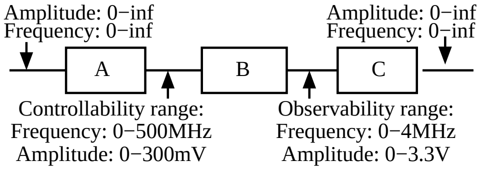

Figure 2. **Constraints imposed by operation ranges**

The proposed methodology determines these controllability and observability ranges for each point in the system through path traversal by utilizing the operating ranges and behavioral models of the blocks in the system as shown in Figure 2. The traversal starts at the primary inputs and outputs. As each basic block is traversed, the limitations imposed by this block on the signal attributes are recorded as constraints. The mappings between the signal attributes at each intermediate point and the signal attributes at the primary pinouts are also recorded. These mappings are subsequently used to compute the accuracy of the tests and to determine the test signal attributes at the primary pinouts once a particular test is generated.

Due to non-idealities of analog modules, noise and harmonic components impose additional system level constraints. If test signals fall below the noise level or coincide with harmonic components, the test information is degenerated. In order to avoid such degeneration, the position of the harmonic signals and the noise level in the system needs to be determined. The proposed tool conducts a worst case noise analysis from the primary input to the primary output to determine the minimum detectable signal level. Since the position of the harmonic components depends on the input signal frequencies, the tool keeps a list of harmonics in terms of the input signal, which are imposed as forbidden regions when the signal attributes are set.

4.2 Modeling Issues

Any dynamic analog signal can be reconstructed in the time or the frequency domain by its frequency, amplitude and phase. However, these three basic attributes are not sufficient to model signals due to non-idealities in the circuits or environment. Each signal is accompanied with unwanted components such as noise or spurious response. If the desired signal cannot be differentiated from these unwanted components, test information will be lost.

Unwanted Signals: In the context of test generation and fault simulation, unwanted signals can be classified as noise or harmonic components. In order to preserve test related information, additional constraints are imposed on test signals due to such non-ideal components.

The exact amplitude and phase information of noise is not available. However, its power spectral density or its total power in a given bandwidth can be computed. During path traversal, the noise level in the system is tracked and test signals are restricted to above the noise level.

The power of harmonic components, on the other hand, is hard to predict. These components are either generated from input tones or by clocked operations. As a result, their frequency information is available as a function of input and clock frequencies. This information is tracked during path traversal and test signals are set so as not to coincide with these frequencies. Figure 3 illustrates the constraints on test signals due to unwanted signals.

Clock operation at 400kHz generates the harmonic components in Figure 3. The desired signal at 100kHz satisfies both observability requirements such that it will not coincide with any clock harmonics and that it be above the noise floor corresponding to 2MHz bandwidth and 4K samples.

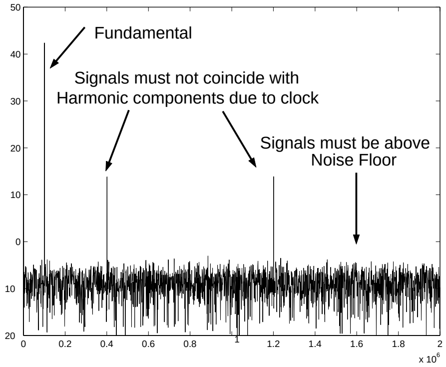

Figure 3. **Constraints imposed by noise and harmonics**

Behavioral Library: Within a given operation range, the input-output behavior of a basic block can be expressed with simple linear relations. Outside this operation range, there exists a transition range where the block produces some output, but the attributes are severely dependent on process variations. Therefore, this region provides little or no information. The traversal scheme restricts test signals to be propagated through operation ranges only.

The ideal behavior of a basic block is not sufficient to reason about complications that have an impact on test signals, such as noise or harmonics. Therefore, such expected non-idealities are also included in the library models.

4.3 Requirement Library

System specifications define the shape of the output signal based on a given input signal. For each specification, the input space can be partitioned into regions where the dependency of the output signal attributes on the specification can be expressed in simple terms. The requirement on the specified parameter can then be imposed on the output signal attributes. For example, the 1dB compression point (P_{1dB}) specification for a mixer imposes no requirement on the gain of the mixer for low input signal amplitudes. As the input signal is increased to near P_{1dB}, some compression in gain is tolerated. At P_{1dB}, the allowable gain compression is exactly 1dB. Intuitively, the ideal test for this specification has an amplitude of P_{1dB} and checks whether the gain has been reduced by more than $1dB$. In an integrated environment, the amplitude of P_{1dB} may not be available due to operation range restrictions of other components. In this case, lower amplitudes may still provide some coverage for the P_{1dB} specification. Therefore, test signal attributes for a certain specification need to be determined after system level constraints have been computed.

Test Signal Attributes	Requirement
$f_{in} \in \{f_{pb}\}$ $P_{1dB}-$1dB$< A_{in} < P_{1dB}$	$A_{out} > G_M + P_{1dB} -$1dB $-$ $k*(P_{1dB} - A_{in})$
$f_{in} \in \{f_{pb}\}$ $A_{in} = P_{1dB}$	$A_{out} > G_M + P_{1dB}-$1dB

Table 1. P_{1dB} **Requirements**

Table 1 shows the requirements for the P_{1dB} specification. The first row of the table defines signal attributes that are higher threshold, but still lower than P_{1dB}. Parameter k serves a first-order approximation of the gain compression curve, as shown in Figure 4. This approximation is only valid for a small region, as given in Table 1. Clearly, variations associated with the introduced parameter k decrease the test accuracy for this input partition.

The second partition in Table 1 has the least dependency on circuit parameters other than P_{1dB}, and therefore is the ideal test input. If this amplitude level cannot be attained due to system level constraints, P_{1dB} can be tested using the first partition with compromised accuracy. In this case, only the first partition is propagated to the primary output. If signals corresponding to both partitions can be propagated to the primary output, test accuracy computation takes variations in circuit parameters into account so as to select the input partitions with the highest accuracy.

In most cases input signal definitions corresponding to the selected partition provide some flexibility in terms of setting the signal attributes. As an example, if the first row of Table 1 is selected to test the P_{1dB}, the frequency of the signal can be set anywhere within the pass-band. Similarly , the amplitude of the signal can be set anywhere within the range overlap between the attainable signal level and input definition. This test can be combined with other tests as long as there is an overlapping region, as shown in Figure 5. Thus, after all tests have been generated, overlapping regions between tests are determined. Test signal attributes are set to the mid-point of such overlapping regions providing test compaction without fault coverage loss.

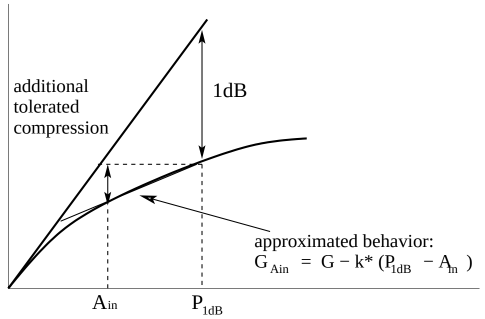

Figure 4. Approximate gain compression behavior

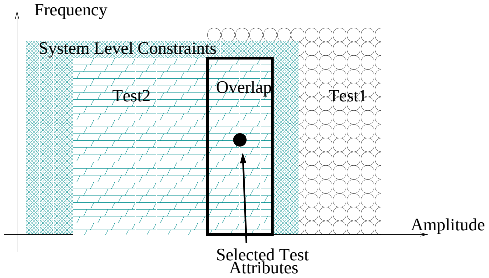

Figure 5. Merging Input Signals of Distinct Tests

5 Fault Simulation and Test Evaluation

Additional test compaction can be attained by compromising fault coverage. The test generation algorithm aims at maximizing the fault coverage of each parameter. However, a test generated for one parameter can provide adequate coverage in terms of several other parameters even if no overlap can be attained between the generated tests. Fault simulation can be utilized to identify such cases and enable further test compaction.

Fault simulation aims at computing the level of misclassification for a parameter when a test input is specified. The proposed fault simulation tool makes use of the same response database to define the requirements for each parameter. If all the chips with acceptable parameters satisfy and all the chips with unacceptable parameters fail the requirements at the primary outputs, the fault and yield coverages will both be 100%. Frequently, the requirements involve other circuit parameters. Since the exact values of these parameters are not known, their nominal values are used in the extraction and propagation of the requirements. The difference between the real and nominal values of these parameters causes misclassification. While such misclassification is unavoidable whenever tolerance and noise effects hold, we proceed to show an estimation method for identifying the extent of such misclassification in order to enable selection of the appropriate tests.

For a specific parameter, p, a fault-free chip is rejected if the variations in other parameters result in the output requirement, r, not being satisfied. Therefore, the probabilities of rejecting a chip with a fault-free p and accepting a chip with a faulty p are:

$$\frac{P(p_{min} < p < p_{max})}{Y_p} \cdot (P(r \leq r_{min}) + P(r \geq r_{max}))$$

$$\frac{P(p_{min} > p) + P(p > p_{max})}{1 - Y_p} \cdot P(r_{min} < r < r_{max})$$

where Y_p is the yield of the parameter, p.

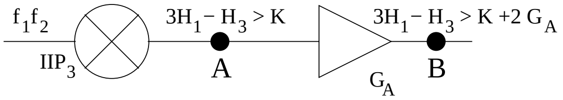

Figure 6. IIP_3 **Requirement and its Propagation**

As an example, consider the mixer IIP_3 as in Figure 6. The requirements at Points A and B are:

A: $3H_1 - H_3 > 2(IIP_{3_{min}} + G_M)$
B: $3H_1 - H_3 > 2(IIP_{3_{min}} + G_M + G_A)$

As a result, coverages are given by the following relation:

$$FC = 1 - \frac{\int_0^{\infty} P(IIP_3 = IIP_{3_{min}} - x) \cdot P(G > G_{nom} + x) \cdot dx}{1 - Y_{IIP_3}}$$

$$YC = 1 - \frac{\int_0^{\infty} P(IIP_3 = IIP_{3_{min}} + x) \cdot P(G < G_{nom} - x) \cdot dx}{Y_{IIP_3}}$$

where $G = G_M + G_A$

In the above equations, the third harmonic is assumed to be above the noise level for simplicity. The distribution of the composite parameter, G, is computed out of the given distributions of G_M and G_A:

$$\mu_{(G_A+G_M)} = \mu_{G_A} + \mu_{G_M};\ \sigma_{(G_A+G_M)} = \sigma_{G_A} + \sigma_{G_M}$$

5.1 Test Set Compaction

The proposed tool computes the fault and yield coverages of a given set of tests for the targeted parameters in the system. Some tests may provide better coverage for a particular parameter but may result in poor coverage for another parameter. In order to provide a better evaluation, the fault and yield coverage results need to be composed for a given test. For two parameters that are tested with the same test input, coverages can be combined with the following relations.

p_1 and p_2 requirements inversely correlated:

$$YC = 1 - (1 - YC_{p_1}) - (1 - YC_{p_2})$$

$$FC = 1 - (1 - FC_{p_1}) - (1 - FC_{p_2})$$

p_1 and p_2 requirements not correlated:

$$YC = 1 - (1 - YC_{p_1}) \cdot YC_{p_2} - (1 - YC_{p_2}) \cdot YC_{p_1}$$
and
$$FC = 1 - (1 - FC_{p_1}) \cdot FC_{p_2} - (1 - FC_{p_2}) \cdot FC_{p_1}$$

p_1 and p_2 requirements directly correlated:

$$YC = min(YC_{p_1}, YC_{p_2})$$

$$FC = max(FC_{p_1}, FC_{p_2})$$

6 Experimental Results

The proposed methodology is applied to an IF receiver path as shown in Figure 7. The system has a 60dB dynamic range with the minimum sensitivity level of -67dBm. The path gain is set to 30dB, as the gain control is done in the RF stage. The local oscillator frequency is at 50MHz; the continuous-time filter has a cut-off frequency of 350kHz. The 10-bit ADC has a maximum sampling rate of 5MHz.

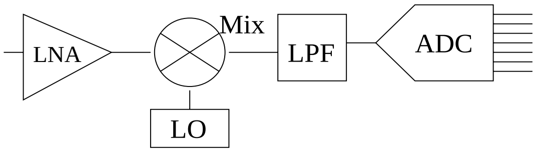

Figure 7. **IF receiver channel used in the experiment**

For the experiment, four distinctive specifications, the third order input intercept point (IIP_3) and the 1-dB compression point (P_{1dB}) of the mixer, the cut-off frequency (f_c) of the low-pass filter, and the total harmonic distortion (THD) of the sigma-delta ADC are studied. The specifications and the parameter distributions are given in Table 2.

Spec	Requirement	Nom	σ
$THD <$	-60dB	-64.2dB	1.8dB
f_c	350kHz	350kHz	8.8kHz
$P_{1dB} >$	315mV	330mV	7mV
$IIP_3 >$	16dBm	19dBm	1.6dBm

Table 2. **Targeted system specifications**

Table 3 shows the ranges of test signals that can be propagated from the primary input to each basic block. For simplicity, only one-tone signals are included in the table. Similar input ranges with more complicated intermodulation harmonics are also computed for two and three-tone signals. The intersection of these propagatable ranges with each test input partition pinpoints the possible test ranges for that partition. Partitions that lead to zero test range are dropped from the computation as these signals cannot be propagated from any system inputs. Test accuracies for the remaining partitions are computed and the partition that leads to the highest accuracy is selected as the test signal.

Table 4 shows the requirements for the selected test partitions. The test signal and response for THD need to lie

Ranges	A	B	C
Freq	(0,55)MHz	(0,50)&(50,105)MHz	(0,337.5)kHz
Level	(-74,2.5)dBm	(-49,12.5)dBm	(0.89, 3)V
Phase	(0,II)	NA	NA
Noise	-77dBm	-52dBm	1.77mV
Spurs	$\{\}$	$\{nf_1 - mf_2\}$	$\{nf_1 - mf_2\}$

Table 3. Propagatable Signals

Spec	Requirement
THD	$(H_3+H_5+H_7)_{f_1}+(H_9+H_{11}+H_{13})_{f_2}-H_1<60\text{dB}$
f_c	$G_{pb}-G_1<3dB, G_{pb}-G_2>3\text{dB}$
P_{1dB}	$A_o>G_M+(1-k)\ 2.97\text{dBm}-1\text{dB}+kA_1$
IIP_3	$3H_1-H_3>32\text{dB}-G_M$

Table 4. Requirements for selected input partitions

within the passband of the ADC converter whereas the odd order harmonics generated by the mixer need to lie within the stop-band of the filter to prevent the mixer harmonics from corrupting test information. The methodology selects a two-tone signal as no single-tone signal satisfies these conditions. For the f_c test, a two-tone signal is selected, as the composite pass-band gain needs to be measured as a system level parameter. For P_{1dB}, the input power is set to the highest propagatable input level to reduce the dependency on parameter k. After mapping the block inputs to system inputs, the attributes of the system level tests are set to the mid-point of the test ranges. The resulting test input attributes and corresponding test accuracies are given in Table 5.

Spec	Test	Err	Misclass
THD	-8.05dBm & 50.311MHz -8.05dBm & 50.096MHz	5dB	2.2%
P_{1dB}	-7.75dBm & 50.25MHz	0.6dB	7.9%
IIP_3	-11.1dBm & 50.133MHz -11.1dBm & 50.201MHz	0.6dB	5.6%
f_c	-11.1dBm & 50.311MHz -11.1dBm & 50.096MHz	0dB	0%

Table 5. Test Signals and Accuracy

Misclassification probabilities with the pass/fail threshold set at the specification threshold are also given in Table 5. For loose specifications, at the expense of increasing the misclassification rate for faulty parameters, the pass/fail threshold can be adjusted so that there is no misclassification for fault-free parameters. Similarly for tight specifications, the threshold can be adjusted to decrease the misclassification rate for faulty parameters.

In this example, no test overlap is observed, due to the distinct nature of the targeted parameters. However, fault simulations indicate that the test generated for IIP_3 results in a misclassification rate of 6.4% for the cut-off frequency of the filter. If this misclassification rate is tolerable, the test input for f_c can be changed to this test input, thus reducing the number of required tests by one. This reduction results in appreciable savings in terms of test time since a f_c test requires about 4K samples and FFT analysis at the output.

7 Conclusion

Increasing VLSI integration levels necessitate a reevaluation of traditional analog test techniques, reliant on dedicated block access for test. Not only are such traditional techniques inordinately consumptive of area, but they also impact loading and noise characteristics of the design, in the process possibly violating design specifications. System level test design that proceeds in parallel with the circuit design is the only viable solution to avoid last-minute DFT insertions.

We propose and illustrate herein new approaches that automatically generate and compact system level tests. Testability problems are also reported in terms of inadequate test accuracy and inability of providing required test signals to a certain basic block.

In order to evaluate the efficacy of the proposed tool, several parameters of distinct DC and intermodulation behavior are considered. The results indicate not only that automated test generation for analog circuits is feasible, but also that it can provide great reduction in test time. The simultaneous multiple specification targeting we outline in the proposed tool helps ensure significant test compaction which would be impossible in an isolated block-based test environment.

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