

Automated Test Development and Test Time Reduction for RF Subsystems

Sule Ozev
CSE Department
UC San Diego
La Jolla, CA 92093
sozev@cs.ucsd.edu

Alex Orailoglu
CSE Department
UC San Diego
La Jolla, CA 92093
alex@cs.ucsd.edu

Hosam Haggag
National Semiconductor
Santa Clara 95051
hosam.haggag@nsc.com

Abstract

Increasing percentage of test cost within the overall manufacturing cost for RF sub-systems results in a need for new, low-cost, and efficient test development methods. A methodology for automating test development for RF systems is presented. Test time reduction is achieved by selecting test signal attributes that can target several parameters at once. Due to its high computational efficiency, the tool can be applied multiple times at early design stages; thus enabling parallel test and design flow.

1 Introduction

Due to the lack of new methodologies in test development to keep up with the increasing levels of integration, test cost constitutes a growing percentage of overall manufacturing cost for RF subsystems. The current industrial practice of testing RF subsystems consists of providing external I/O access to each module and conducting the test of each module in an isolated fashion. As the size and number of basic blocks in a typical system increase, such a test approach results in unacceptably high test overhead in terms of area, performance and test time. New system level approaches may provide great reduction in test time and performance overhead by compacting the test set and eliminating unnecessary test points.

Several system-level test development approaches have been proposed for RF subsystems. In order to extract a set of performance parameters, a self-test strategy that utilizes sampled IQ modulation is presented in [1]. Most critical specifications, such as phase noise, blocker performance, and linearity cannot be tested with this strategy as it would require extraction of these parameters from the bit error rate (BER). Similarly, the authors discuss an overall approach to test the design of communication circuits with little emphasis on the measurement of radio-frequency specifications [2].

The automation efforts in the analog test area rely on detailed circuit simulators, such as SPICE. A number of approaches utilize the sensitivity of measurable parameters to circuit components and aim at determining the test input that maximizes this sensitivity [3, 4, 5]. The sensitivities are determined through multiple SPICE simulations. Such approaches have very little applicability in the RF domain. Important RF parameters, such as phase noise or linearity, are

hard to model at the transistor level. In addition, transistor level analysis requires high simulation times and therefore is not efficient.

In order to prevent the test overhead, test development needs to be incorporated into the design flow. In [6], a test plan development and testability analysis example is given for Bluetooth transceiver subsystems. In this work, a generic architecture is chosen to illustrate test development at the system level. For a given RF system, various architectures and implementation styles are available. In order to analyze a number of possibilities for test generation and test set size reduction at various design stages, efficient automated tools are needed.

This paper presents a methodology for automated test plan development and test time reduction. Test generation aims at determining the attributes of test signals and measurement methodology for a given set of circuit specifications. System level constraints are determined through a library-based analysis, utilizing operating range behavioral models, parameters, their tolerances and expected non-ideal behavior.

In some cases, there may be overlaps in terms of test needs of several parameters. Selecting the input signal attributes from these overlapping regions enables application of several tests at once, leading to considerable savings in terms of test time. The proposed methodology analyzes the multiple possibilities of testing a targeted parameter and identifies such overlaps to reduce the size of the test set. While high level analysis keeps computational complexity manageable, process variations are incorporated through a probabilistic coverage criterion. Faults in circuit parameters are probabilistically distributed over the entire space.

The next section presents the proposed methodology for test development. Experimental data on several distinct parameters of a receive chain are presented in Section 3 and conclusions discussed in Section 4.

2 Methodology

Specifications of an RF system define certain attributes of the output signal, such as signal-to-noise-ratio, gain, or attenuation, based on the nature of input signals. As an example, for a multi-tone sinusoidal input, the third order input intercept (IIP_3) specification indicates that the third order

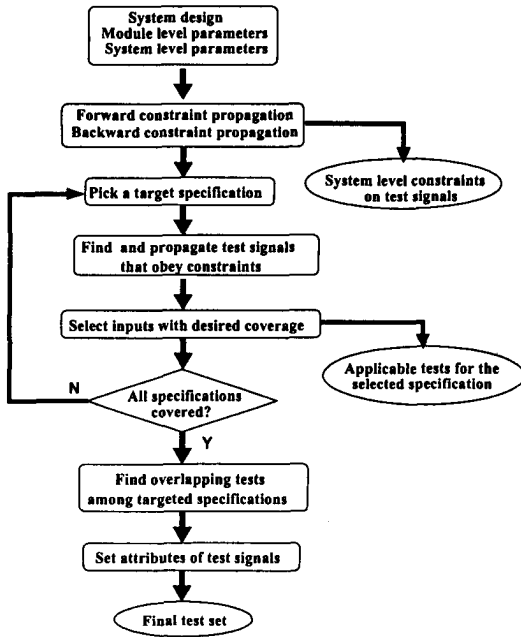


Figure 1. Flow of the proposed tool

harmonic has to be at a certain level depending on the input power and module gain. If the input is a pure sine wave, the IIP_3 specification imposes no requirement on the output signal; thus, such an input provides no test coverage for the IIP_3 specification. For each specification, the input space can be partitioned in such a way so as to describe the output signal requirement imposed by that specification. We call the corresponding portions of the input space *partitions*. Such a database can be utilized to identify the attributes of the test signal that lead to maximum test accuracy for a particular specification.

These partitions basically define certain signal properties, such as its shape or the number of tones, and the ranges of its attributes, such as frequency and amplitude, for which the requirements hold. For most parameters, more than one partition can be defined for distinct input conditions. However, some portion of the input space is not covered by any of the partitions. For such input signals, the targeted parameter has no effect on the output signal; thus there is no need to consider such input signals for testing the parameter. A single-tone signal is an example for such input signals for the IIP_3 parameter.

The proposed tool utilizes a database of partitions, i.e. input signal attributes and corresponding requirements, for selection of test signals and determination of fault-free and faulty responses. The flow of the proposed tool is shown in Figure 1. A first-pass analysis determines the system level limitations on test signals, such as maximum amplitude, resolution, and bandwidth. This one time analysis boosts computational efficiency by avoiding the partitions that cannot propagate through the system. The next step consists of determining the test signals and output requirements that can

Input contains	Requirement
$f_1 \in \{f_{pb}\}$ $f_2 = f_{cmin}$ $f_3 = f_{cmaz}$	$G_1 - G_2 \leq 3dB$ $G_1 - G_2 \geq 3dB$
$f_1 \in \{f_{pb}\}$ $f_{cmin} < f_2 < f_{cmaz}$	$G_1 - G_2 < \log\left(\frac{f_{cmin}}{f_2}\right) * S_{nom} + 3$ $G_1 - G_2 > \log\left(\frac{f_{cmaz}}{f_2}\right) * S_{nom} + 3$
$f_1 \in \{f_{pb}\}$ $f_{cmin} < f_2 < f_3 < f_{cmaz}$	$G_1 - G_2 < \log\left(\frac{f_2}{f_{cmin}}\right) * \frac{G_3 - G_2}{\log(f_3/f_2)}$ $G_1 - G_3 > \log\left(\frac{f_{cmaz}}{f_2}\right) * \frac{G_3 - G_2}{\log(f_3/f_2)}$
$f_2 = f_{cmin}$ $f_3 = f_{cmaz}$	$G_{pb} - G_2 \leq 3dB$ $G_{pb} - G_2 \geq 3dB$
$f_{cmin} < f_2 < f_{cmaz}$	$G_{pb} - G_2 < \log\left(\frac{f_{cmin}}{f_2}\right) * S_{nom} + 3$ $G_{pb} - G_2 > \log\left(\frac{f_{cmaz}}{f_2}\right) * S_{nom} + 3$
$f_{cmin} < f_2 < f_3 < f_{cmaz}$	$G_{pb} - G_2 < \log\left(\frac{f_2}{f_{cmin}}\right) * \frac{G_3 - G_2}{\log(f_3/f_2)}$ $G_{pb} - G_3 > \log\left(\frac{f_{cmaz}}{f_2}\right) * \frac{G_3 - G_2}{\log(f_3/f_2)}$

Table 1. f_c Requirements on the Output Signals

propagate through the system for each targeted specification. Next, test coverage corresponding to each input partition for each targeted parameter is computed and the input partitions that do not provide the desired coverage are dropped. In the test compaction phase, overlaps among test partitions of several parameters are searched. A heuristic algorithm determines the test signal attributes for each targeted parameter so as to minimize the number of tests utilizing the overlaps among the required test signals of several parameters.

2.1 Modeling Test Response and Input Partitions

Each specified parameter of a module imposes requirements on its output signal based on the applied input signal. For the majority of parameters, more than one type of input signal and output requirement can be defined. The purpose of the test generation methodology is to select certain attributes of test signals that can be propagated from the primary input and that yield the desired coverage levels.

In order to enable the selection of such test signals, a database that models the properties of inputs and corresponding output requirements is generated. Table 1 shows the database entries for the cut-off frequency parameter. In order for the cut-off frequency to satisfy its given tolerance, the attenuation at the lower bound of the cut-off frequency has to be no more than 3dB, and the attenuation at the upper bound has to be no less than 3dB. If two signal tones at these boundary conditions and one within the pass-band are available, then the cut-off frequency can be directly tested. If these specific frequencies are not available, due to some system level constraint, the cut-off frequency can be tested using the skirt slope with a different output requirement. The

cut-off frequency test can be conducted either with a single input that contains multiple tones at the desired frequencies, or with single-tone signals applied separately. For parameters that relate to the linearity of the system, such as IIP_3 , a multi-tone signal is required. Such constraints are also indicated within the database.

2.2 Propagation of Requirements to the Output

For each specification, the requirements need to be propagated to the primary output to determine the final pass/fail criterion. The requirements basically indicate a relation among powers of input signal tones and circuit parameters. While propagating the requirement, each tone within the requirement is treated as a signal that passes through modules, such as gain components, filters, and mixers. For example, if the target is the IIP_3 of the mixer shown in Figure 2, the requirement for the given input signal expresses a certain relationship between the first and the third order harmonic. When this requirement is propagated through the amplifier, the gain of the amplifier is used to compute the signal powers at the primary output, thus impacting the requirement. The final pass/fail criterion for the mixer IIP_3 will involve the gain of the amplifier as well.

In the computation of the final pass/fail criterion, the nominal value of the amplifier gain is used. However, the gain of the amplifier may vary within a certain tolerance. Due to the variation in the amplifier gain, some large deviations in the IIP_3 of the mixer may be masked. Similarly, some chips with acceptable IIP_3 may not satisfy the requirement at the primary output. In order to evaluate a given test input, the corresponding fault and yield coverages must be computed.

Computation of test coverages is based on a statistical approach utilizing the distributions of parameters that are involved in the pass/fail criterion for a parameter. Detailed discussion of the test coverage computation is presented in [7].

2.3 Test Compaction

Certain attributes of the required test signals have a flexibility while some may need to have fixed values. As an example, the amplitude of signals in Table 1 can have a wide range, whereas the frequency of test signals for the first and the fourth rows need to be fixed at the boundary conditions. As a result, the input signals corresponding to the propagated

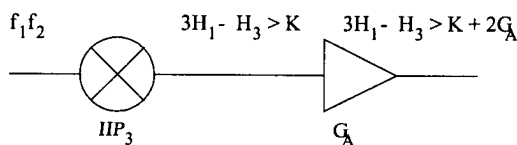


Figure 2. Parameter Requirement and its Propagation

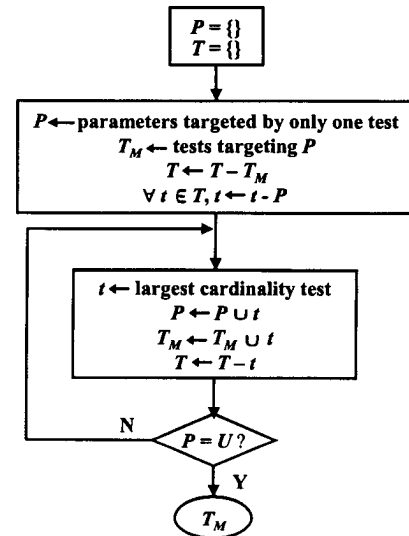


Figure 3. Algorithm for Test Minimization

requirements have some level of flexibility that can be utilized for test compaction without decreasing the test coverage. In most cases, the required test attributes of several parameters may overlap. As analog tests typically require high test times, utilizing such overlaps leads to great reduction in test times.

The test minimization problem can be formulated as a set cover problem: the set of target parameters is called the *universal set*, $U = \{p_1, p_2, p_3, \dots, p_n\}$. Each test t_i represents a subset of the universal set, i.e., it targets one or more parameters. The goal is to find a set of tests, T , with minimum cardinality such that the union of the elements of T equals the universal set. This problem is NP complete; however, with the help of several widely used heuristics, it can be solved in polynomial time. The algorithm for solving the test minimization problem is presented in Figure 3.

First, all parameters that are targeted by only one test are determined. The corresponding tests to these parameters are essential; therefore they are added to the final test list. All additional parameters that are covered with these tests are dropped from the list. After updating the list of so far uncovered parameters for each test, the test that targets the highest number of parameters is selected and added to the list. The algorithm terminates when all the parameters are covered.

3 Experimental Results

The proposed test development methodology is applied to a receive chain shown in Figure 4. The system is designed to have a signal to noise ratio of 15dB at the reference sensitivity level of -80dB. The maximum signal level is at -25dBm. The path gain starts from 40dB and can be increased to 52dB with 5dB coarse and 1dB fine gain steps. System parameters are derived from a global transceiver specification set. For test development, several parameters are targeted: in-band and out-of-band phase noise of the synthesizer, gain attenu-

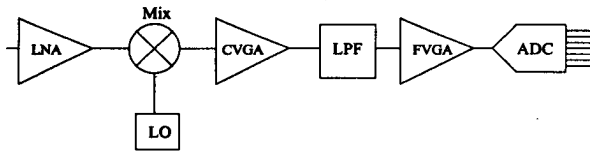


Figure 4. Experimental Set-Up

ations at 1MHz and 2MHz and the cut-off frequency for the channel filter, and third order input intercept of the mixer.

First, all possible test partitions and corresponding requirements are propagated to the primary pinouts for each parameter. After computing test coverages, the test partitions that do not yield at least 90% fault coverage and 95% yield coverage are dropped from the list. In the last phase, overlaps among attributes of several tests are searched and the test compaction algorithm is applied. Table 2 shows the final test set after compaction. Traditionally, each parameter is tested through a separate test. However, test compaction enables testing of six complicated parameters through four test inputs, resulting in a 33% reduction in test time.

The methodology also computes the resulting fault and yield coverages for each parameter. Table 3 shows the test targeting each parameter and resulting fault and yield coverages. The f_c parameter is targeted by two separate tests, *Test1* and *Test2*. Traditionally, the f_c parameter is tested through a multi-tone signal that has one component within the pass-band, one component that coincides with the minimum and one that coincides with the maximum cut-off frequency. However, having all the tones in one signal is not essential to providing coverage for this parameter. As a result, two of the required tones can be coincided with the IIP_3 test, and can be coincided with the in-band phase noise test. In a similar thread, traditionally, both tones of the IIP_3 test are placed within the bandwidth. Since only one fundamental is sufficient to compare with the third order harmonic, it can be combined with part of the f_c test. There are a high number of choices for setting the attributes of the in-band and out-of-band phase noise tests. The basic goal is to have an integrated phase noise that is appreciably above the thermal noise so that the desired coverage levels can be attained. In this example, the in-band phase noise test can be combined with part of the f_c test, and the out-of-band phase noise can be combined with the 1MHz attenuation test.

4 Conclusion

Increasing integration levels for RF systems necessitate a reevaluation of traditional test techniques, reliant on ded-

Test	Attributes
Test1	2-tone ($f_1 \in \{BW\}$; $f_2 = f_{c_{max}}$), -31dBm
Test2	1-tone ($f = f_{c_{min}}$), -31dBm
Test3	1-tone ($f=1MHz$), -28dBm
Test4	1-tone ($f=2MHz$), -28dBm

Table 2. Reduced Test Set

Parameter	Test	FC	YC
IIP_3	Test 1	93%	99%
f_c	Test1, Test2	100%	100%
G_{1MHz}	Test3	99%	100%
G_{2MHz}	Test4	96%	99%
In-band Φ Noise	Test2	96%	100%
Out-of-band Φ Noise	Test3	92%	97%

Table 3. Test Coverages for Targeted Parameters

icated block access for test. Not only are such traditional techniques inordinately consumptive of area, but they also impact loading and noise characteristics of the design, in the process possibly violating design specifications. Perhaps even more problematic is the unnecessary tendency to apply numerous tests, as each block is tested individually, thus additionally consuming precious time on expensive testers. System level test design that proceeds in parallel with the circuit design is the only viable solution to avoid high test times and last-minute DFT insertions.

We propose and illustrate herein new approaches that automatically generate and compact system level tests. Testability problems are also reported in terms of inadequate test accuracy and inability of providing required test signals to a certain basic block.

In order to evaluate the efficacy of the proposed tool, several parameters of distinct nature are considered. The results indicate not only that automated test generation for analog circuits is feasible, but also that it can provide great reductions in test time. The simultaneous multiple specification targeting we outline in the proposed tool helps ensure significant test compaction which would be impossible in an isolated block-based test environment.

References

- [1] M.S. Heutmaker and D.K. Le, "An architecture for self-test of a wireless communication system using sampled IQ modulation and boundary scan", *IEEE Communications Magazine*, vol. 37, n. 6, pp. 98-102, 1999.
- [2] M. Jarwala, L. Duy and M.S. Heutmaker, "End-to-end test strategy for wireless systems", in *ITC*, pp. 940-946, 1995.
- [3] N. Hamida and B. Kaminska, "Analog Circuit Testing Based on Sensitivity Computation and New Circuit Modeling", in *ITC*, pp. 652-661, 1993.
- [4] M. Slamani, B. Kaminska and G. Quesnel, "An Integrated Approach for Analog Circuit Testing with a Minimum Number of Detected Parameters", in *ITC*, pp. 631-640, 1994.
- [5] K. Saab, N. Ben-Hamida and B. Kaminska, "Parametric Fault Simulation and Test Vector Generation", in *DATE*, pp. 650-656, 2000.
- [6] S. Ozev, Christian Olgaard and A. Orailoglu, "Testability Implications for Low-cost Integrated Radio Transceivers: A Bluetooth Case Study", in *ITC*, November 2001.
- [7] S. Ozev and A. Orailoglu, "Test Selection Based on High Level Fault Simulation for Mixed-Signal Systems", in *VTS*, pp. 149-154, 2000.