

# Multilevel Testability Analysis and Solutions for Integrated Bluetooth Transceivers

**Sule Ozev**

University of California at San Diego

**Alex Orailoglu**

University of California at San Diego

**Christian V. Olgaard**

LitePoint

As use of wireless communications rises and profit margins shrink, low-cost solutions are becoming increasingly important. Incorporating test design and DFT into the system design flow is essential to achieving such solutions. This case study analyzes test requirements, implications, and test cost for low-cost Bluetooth systems, which enable communication among several electronic components.

■ **WIRELESS COMMUNICATIONS** are becoming the norm for information transmission. Stringent market requirements and tight time-to-market windows call for low-cost RF subsystems. Traditional design flows for an RF transceiver focus on minimizing system hardware cost, and test design typically begins when system design is about to end. However, decreasing profit margins and increasing chip production costs are elevating test-related expenditures to an ever-larger percentage of overall manufacturing cost. Because of poor testability, the system with the lowest hardware cost might

not have the lowest overall cost. To achieve optimal solutions, designers must incorporate test considerations into the overall design flow.

Bluetooth, an increasingly popular radio transceiver standard, enables communication among several of today's popular electronic components, such as personal digital assistants and microwave ovens.<sup>1</sup> Because Bluetooth is not the main feature in these components, achieving overall low cost is essential to getting a market share. For example, a radio subsystem's target market value is \$2.50 with a 50% margin, implying a tolerable \$1.25 for a packaged and tested transceiver chip.

To enable design optimizations that lead to low-cost architectures, Bluetooth's RF specifications are fairly relaxed compared to those of other standards, such as the Global System for Mobile Communications (GSM) and code division multiple access (CDMA). However, the same set of specifications needs to be tested regardless of how relaxed those specifications might be. Because of decreasing profit margins, finding a cost-effective way for testing is increasingly more important for Bluetooth transceivers.

To keep test cost within acceptable bounds, designers must begin analyzing system testability during the early design stages. They must address testability problems before fully freezing the architecture and specifications.

Designers need to implement appropriate DFT changes to solve these problems. They should also incorporate tester equipment cost and test time into their analyses.

DFT solutions are not necessarily confined to adding hardware components, such as test buses and multiplexers, to simplify testing. The best DFT solution can inherently change the underlying system architecture or adjust the system specifications not only to ease test application but also to lower tester cost.

To measure a system's performance parameters, Heutmaker and Le presented a self-test strategy that uses sampled IQ modulation (where "I" is the in-phase component, and "Q" is the quadrature component).<sup>2</sup> However, this strategy cannot measure most critical specifications, such as phase noise, blocker performance, and linearity. Doing so would require duplicating complicated signal interactions and extracting these parameters from the measurable bit error rate. In addition, BER typically requires long test times. Moreover, BER is often difficult to measure correctly, because it is very sensitive to power level. Similarly, Jarwala, Duy, and Heutmaker discussed an overall approach to test the design of communication circuits with little emphasis on measuring RF specifications.<sup>3</sup>

Our goal here is to show how to incorporate testability analysis into the design flow at early stages and thus provide low-cost test solutions. To do so, we analyze testability tradeoffs for a radio system at multiple levels, such as architecture selection, parameter translation, and basic-block implementation. We chose Bluetooth transceiver systems with no I/O access to internal blocks for this test analysis because such system-level approaches provide lower-cost testing compared to isolated module-based testing, which requires the addition of test points and leads to high test times. At the system level, we discuss design and test tradeoffs for various architectures commonly used for Bluetooth. But because an examination of testability considerations at a lower level requires elaborating on a concrete architecture, we narrow our focus to receiver architectures that employ a digital demodulator using an A/D converter (ADC).

## Bluetooth architecture considerations

For all wireless systems, test considerations should run in parallel with design considerations. Low-cost wireless solutions must employ the architecture with the lowest possible production cost, meaning they must use minimal external components of the smallest possible die area and the lowest possible test cost. But to be viable, the chosen architecture must provide a maximum level of integration along with full incorporation of the system's particular design requirements.

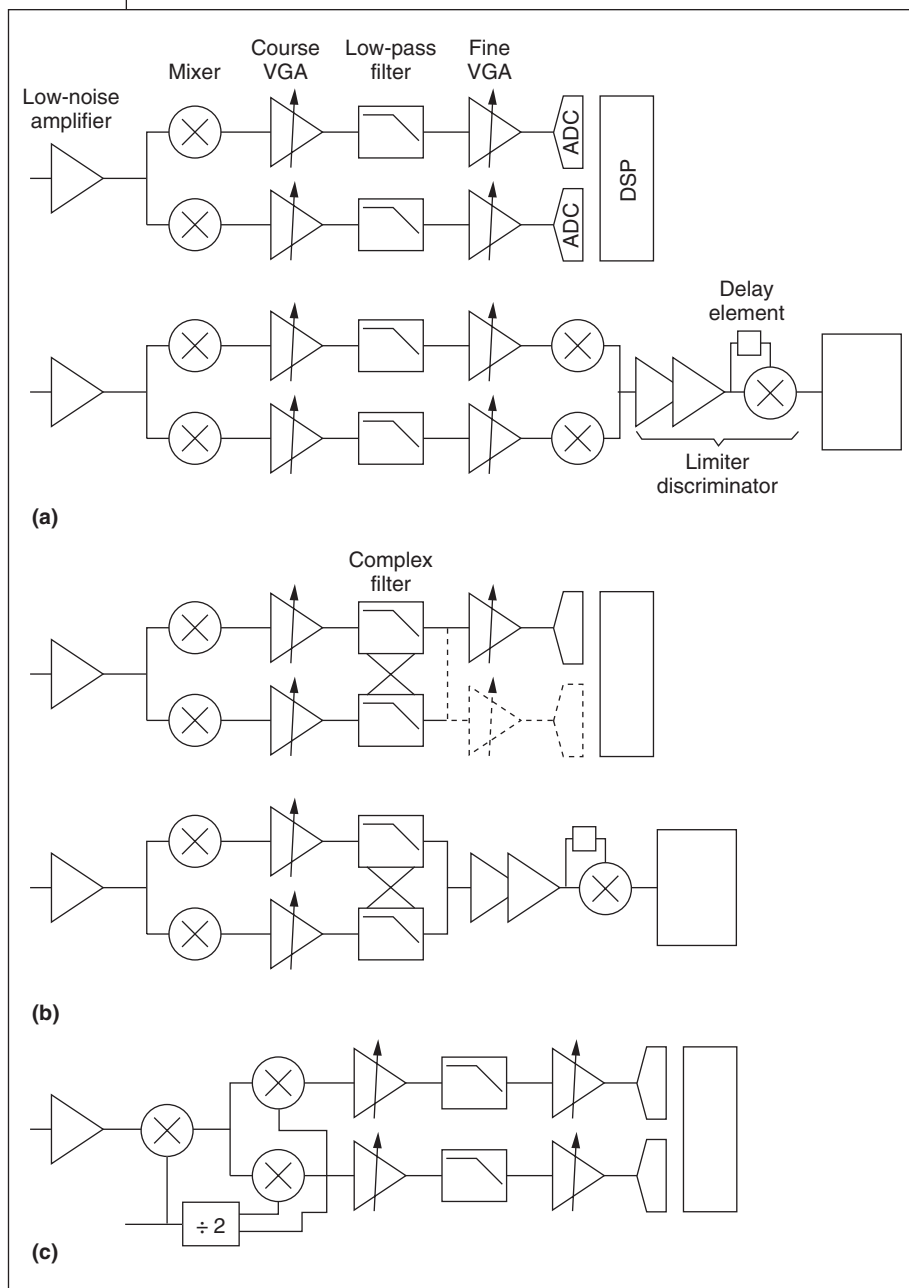
Bluetooth's time division duplex (TDD) property enables decoupling the transmitter from the receiver architecture; the two architectures then only need to share the frequency synthesizer. Such decoupling enables highly optimized architectures for receiver and transmitter operations.

### Receiver architectures

Figure 1 (next page) shows three types of receivers that designers generally use to achieve the desired level of integration. A receiver with an intermediate frequency of 0 (zero-IF receiver) converts the desired channel directly down to base band in IQ format. A low-IF receiver converts the desired channel down to a frequency close to base band and demodulates the data at this frequency. A wide-IF receiver uses a higher intermediate frequency that cannot be directly digitized, and thus requires double conversion.

From a filtering perspective, true zero-IF receivers are optimal because simple low-pass filters at half the channel bandwidth provide channel selectivity. However, the dc offset sensitivity of true zero-IF receivers make their design challenging. Offsets appear as part of the desired signal, and large dc offsets can saturate the complete receiver chain, generating high BERs. Moreover, because such receivers convert the desired channel directly to base band, the flicker noise ( $1/f$  noise) can be significant enough to degrade the receiver's sensitivity.

Using a low-IF rather than a true zero-IF receiver alleviates many of these drawbacks. Because low-IF receivers convert the desired signal to an IF rather than to dc, flicker noise



**Figure 1. Possible receiver architectures: zero-IF (a), low-IF (b), and wide-IF (c).**

and DC offsets are out of band. However, the mixer's image falls in band, so using a low-IF frequency requires significant image rejection, necessitating the use of complex filters that consume power and die area.

The low-IF receiver is a special case of a traditional superheterodyne receiver (which uses an intermediate frequency for down conversion). You could use a superheterodyne receiver without introducing channel selectivity (the

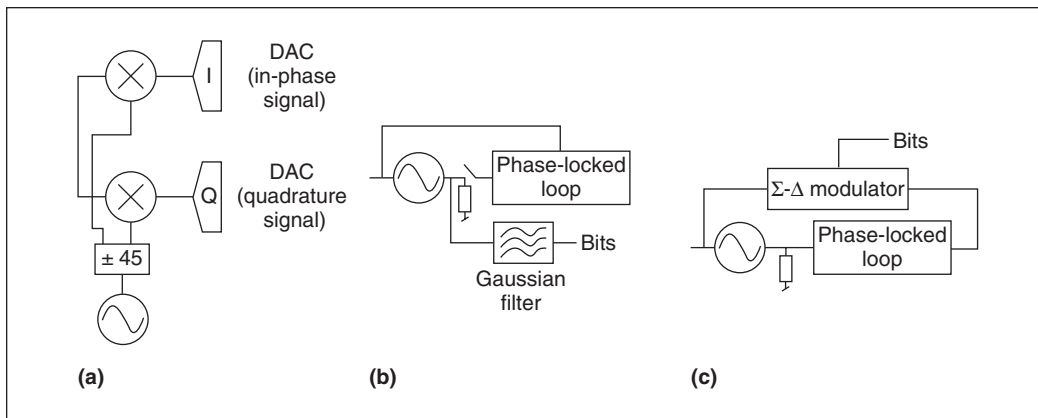
ability to filter and amplify the desired signal while suppressing the signals that fall out of band).<sup>4</sup> If you use a wide-IF receiver, the image moves out of band, so the front-end filter attenuates the image. A double conversion is then necessary, requiring two mixers and increasing the linearity requirements and power consumption. Having receiver and transmitter chains share a single voltage-controlled oscillator (VCO) can reduce power consumption.<sup>5</sup> For wide-IF receivers, the second mixer shown in Figure 1 usually converts the IF signal directly to base band, thus obviating local-oscillator leakage to the antenna. Unfortunately, for both low- and wide-IF receivers, VCO sharing eliminates the possibility of true loop-back simple signals.

#### Transmitter architectures

To optimize die size, designers often have the transmitter and receiver share the frequency synthesizer. Consequently, the transmitter architecture must use a synthesizer frequency in the range required for the receiver.

Because Gaussian frequency shift keying (GFSK) has no envelope information, a traditional transmitter architecture, shown in Figure 2a, is perhaps overkill for Bluetooth in terms of design cost. Designers typically use direct VCO modulation that eliminates the two D/A converters and the multibit signal-processing unit driving them.

A typical approach to GFSK modulation is to use an open loop to modulate the VCO,<sup>6</sup> as Figure 2b shows. Initially, the control hardware locks the VCO to the center of the desired transmitter frequency. After opening the synthesizer loop, this hardware applies data directly to the VCO through a Gaussian filter. This low-cost approach has some significant problems in terms of satisfying both specifications and testability.



**Figure 2. Possible transmitter architectures: quadrature modulation (a), open-loop voltage-controlled oscillator (VCO) modulation (b), and closed-loop VCO modulation (c).**

For one, the synthesizer loop must exhibit very low leakage to meet Bluetooth's frequency drift requirements, making the system sensitive to process variations. Both frequency pushing and drift decrease test accuracy because they cause a difference between the actual operating frequency and the frequency used in test computations. A possible but slightly more complex solution is closed-loop VCO modulation, which Figure 2c shows. Among the many existing approaches for closed-loop modulation,  $\Sigma$ - $\Delta$  modulation within the synthesizer is the most promising. Although this architecture gives a more robust solution in terms of process variations and frequency drift, engineers still need to measure the loop's phase noise, both in and out of band.

Direct VCO modulation—both open and closed loop—severely complicates the feasibility of performing a true loop-back test on the system. The problem is the modulation of the local oscillator that drives the receiver's down-conversion mixer. Naturally, the system is not intended to operate simultaneously in transmitter and receiver mode. However, using a loop-back path in test mode would let engineers perform all the tests at low frequencies, reducing tester cost.

#### Selected transceiver architectures

To enable a lower-level analysis, we need to concentrate on a concrete architecture. So we focus on VCO modulation transmitters and low- and wide-IF receivers. The transmitter test

focuses on testing the transmitter mask, phase error, frequency drift, noise performance, and in-band spur levels.

On the receiver side, we consider a more block-based approach and focus on filter characterization, VCO phase noise, phase-locked loop (PLL) phase noise, and a third-order input intercept.

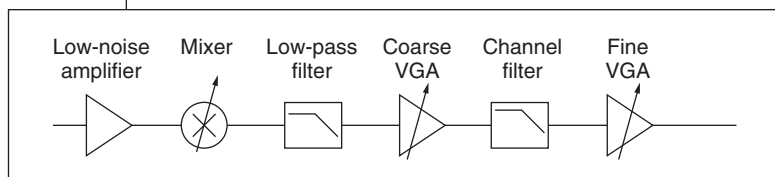
#### Bluetooth specifications

Regardless of the underlying architecture, any Bluetooth system must satisfy certain minimum RF performance requirements. Although the specifications relate to full transceiver performance, it is possible to break them down to radio and radio sub-block performance requirements.

#### Receiver specifications

Bluetooth's reference sensitivity exceeds  $-70$  dBm, and the maximum signal level is  $-20$  dBm, yielding a minimum dynamic range of 50 dB. The thermal-noise level at the primary input is  $-114$  dBm with a 1-MHz double-sided bandwidth. Assuming the demodulator requires a signal-to-noise ratio (SNR) of 15 dB, the path's noise figure must be less than 29 dB.

The blocking scenarios in the RF specification define the channel sensitivity.<sup>1</sup> The filter must suppress the given blocker to a level at which an SNR of 15 dB is possible. At the 1-MHz offset, the blocker has the same power as the desired signal; thus, it must be attenuated by 15 dB. At the 2-MHz offset, the blocker is 30 dB above the desired signal, requiring a



**Figure 3. Generic receiver architecture.**

45-dB attenuation. Similarly, a 3-MHz offset requires a 58-dB attenuation.

We can derive linearity requirements from the blocking specifications. Two strong out-of-band signals, spaced by frequency  $f$  and  $2f$  from the desired signal, cause in-band interference at frequency  $f$ , such that

$$\begin{aligned} |f_1 - 2f_2| &= |f_{\text{desired}} \pm 2f_{\text{offset}} - 2(f_{\text{desired}} \pm f_{\text{offset}})| \\ &= f_{\text{desired}} \end{aligned}$$

We derive the third-order input intercept ( $IIP_3$ ) requirement as follows:

$$IIP_3 > \frac{3P_{f_{1,2}} - (P_{\text{ref}} + 6\text{dB} - SNR - 2\text{dB})}{2}$$

or

$$IIP_3 > -20 \text{ dBm}$$

where  $P_{f_{1,2}}$  is the blocking signal power, and  $P_{\text{ref}}$  is the reference sensitivity level.

Although the receiver chain's complete dynamic range is 50 dB, we can relax the ADC's

dynamic range requirements using the amplifiers' variable gain control. If the ADC's thermal-noise floor is at least 10 dB below the accumulative noise, and the required fading margin is 6 dB, then the desired dynamic range is 25 dB. Therefore, a 5-bit ADC, providing a 30-dB dynamic range, is adequate to meet the minimum specifications.

To enable a discussion of the testability problems and test solutions, we analyze a generic receiver architecture, like the one shown in Figure 3, to derive a set of parameters. Table 1 gives the set of resulting specifications for the receiver chain analysis. The mixer has a 5-dB range for adjustable gain, whereas the range for both the coarse and fine variable gain amplifiers (VGAs) is 10 dB.

Transmitter and synthesizer specifications

Most requirements on the transmitter side rest on the synthesizer components, the PLL and the VCO, because the transmitter circuit consists mainly of these two crucial elements. The transmitter power spectrum must be 20 dB below the carrier (the basic transmitted signal) at the bandwidth edge. Bluetooth specifies out-of-band spectrum power as  $-20$  dBm at a 2-MHz offset, or  $-40$  dBm at 3 MHz.

In a transmitter architecture using VCO modulation, the VCO is the dominant contributor to adjacent channel noise. Assuming the transmitter spectrum's 3-dB bandwidth is about

**Table 1. Design and testability summary of receiver architectures.**

Bluetooth component	Typical gain (dB)	Maximum actual noise	$IIP_3$ (dB)	Effective $IIP_3$ (dB)	Accumulative gain (dB)	Signal level with typical gain ( $\times 10^{-4}$ )	Noise level with typical gain ( $\times 10^{-5}$ )
Input	0	0 dB	200	200	0	0.707 dB	0.0446 dB
Transmitter/receiver switch	-0.5	0.5 dB	20	20	-0.5	0.668 dB	0.0446 dB
Filter	-3	3 dB	200	200	-3.5	0.446 dB	0.0446 dB
Low-noise amplifier	18	$5 \times 10^{-7}$ V	0	0	14.5	3.540 dB	0.5320 dB
RF mixer	6	$5 \times 10^{-6}$ V	0	0	20.5	7.07 V	1.46 V
Low-pass filter	-3	$1 \times 10^{-5}$ V	200	200	17.5	5.01 V	1.25 V
Coarse VGA	16	$1 \times 10^{-5}$ V	0	10	33.5	31.60 V	10.10 V
Channel filter	12	$5 \times 10^{-5}$ V	-20	40	45.5	126.00 V	44.90 V
Fine VGA	13	$1 \times 10^{-4}$ V	0	60	58.5	562.00 V	205.00 V

400 kHz off center, we add a correction factor of  $10 \log(800 \text{ kHz}/100 \text{ kHz}) = 9 \text{ dB}$ , and a margin of 3 to 6 dB. Thus, the required VCO phase noise,  $\Phi_n(f)$ , is  $-123 \text{ dBc/Hz}$ . On the receiver side, we use the blocker specification and the following equation to determine the VCO's phase noise requirements:

$$\Phi_n(f) = P_{\text{blocker}} - P_{\text{desired}} - \text{SNR} - 3 \text{ dB} - 10 \log(BW)$$

where  $BW$  is the synthesizer loop bandwidth. Combining the two phase noise requirements and a  $1/f^2$  frequency roll-off for the VCO gives  $-114 \text{ dBc/Hz}$  for the 1-MHz reflection of the phase noise requirement. The RMS phase error specification imposes a limit on the synthesizer noise. In closed-loop modulation, this is the in-band PLL phase noise; for the open loop modulation, this limit is the VCO phase noise. To achieve symbol jitter better than  $1/8$  of the symbol time, the in-band noise floor must be around  $85 \text{ dB/Hz}$  below the carrier.

### Specification-based tests for Bluetooth

We focus on the Bluetooth specifications that are most likely to induce testability problems, and we analyze the relevant test requirements. This analysis assumes that test application is at the system level; that is, no access to the system's internal points exists. Therefore, we observe the results at the ADC outputs. The goal is to test the system using a single, simple source, thus minimizing the need for RF test equipment.

#### Filtering characteristics in the receiver path

The filtering characteristics on the receiver path basically stem from the blocker and minimum SNR requirements. From the required attenuation levels, we derive the filtering characteristics shown in Figure 4.

The simplest way to ensure the filter meets these requirements is to follow the points of the blocker specifications and apply a multitone sinusoidal waveform to the system. The next step is to compare the gains at these specific frequencies to the pass-band gain and make a pass/fail decision regarding the attenuation. A

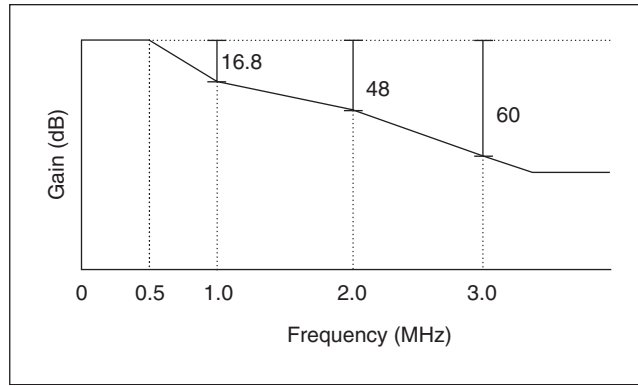


Figure 4. Required filter roll-off.

Table 2. Blocker test signal level.

Signal	ADC input signal level (mV)	
	Under normal gain	Under increased gain
Desired	188.0	188.0
At 1-MHz offset	43.1	188.0
At 2-MHz offset	2.7	16.6
At 3-MHz offset	0.7	4.3
Thermal noise	1.7	3.5

multitone signal is difficult to generate at the desired frequency (2.5 GHz). It is also difficult to observe, because the response at 2 MHz and 3 MHz is likely very small, and using strong signals would probably generate intermodulation.

Optimizing system test results requires using the ADC's full dynamic range. Therefore, it is necessary to use the highest specified input signal power,  $-20 \text{ dBm}$ , because doing so guarantees the receiver's linearity. When such a signal is applied, the variable gain components must remain at their minimum gain (22 dB) until the channel filter is reached, to avoid saturation. However, the channel filter suppresses the blocker test signals. Consequently, it is possible to set the gain of the fine VGA to a higher value for the out-of-band signals, and still not saturate the ADC.

Table 2 gives the ADC input's signal and noise levels under normal and increased gain.

The signal at a 3-MHz offset is near the thermal-noise level. Therefore, we must shift this test in frequency so that the output signal becomes appreciably stronger (at least 3 dB) than the thermal noise. We can then interpolate

the 3-MHz attenuation from the measured data. Such an approach constrains the filter transfer function to have no 0s after the data point; consequently, the skirt slope (the slope of the decrease in gain after the cut-off frequency) does not decrease. This is not a stringent constraint, because the specified frequency is well outside the pass-band range.

A more important test problem pertains to the signal's weakness at 2 MHz. If we use a 5-bit ADC, as suggested earlier, the signal falls below the quantization noise floor. Measuring the attenuation level at a lower frequency offset is not an option, because the filter could have 0s within the band from 1 MHz to 2 MHz. Solving this problem requires a DFT approach.

#### Out-of-band VCO phase noise

Both the receiver and transmitter path specifications impose requirements on the VCO phase noise, because the VCO serves both paths. However, once we determine the VCO specification, we can test this phase noise in either path. The goal is to minimize the number of high-frequency tests, so testing the VCO phase noise in the receiver path is desirable. This path presents the data at base band and thus allows inexpensive postprocessing of data.

We derive the receiver VCO phase noise requirements from the blocking specifications and can perform the test using an out-of-band fundamental signal. Mixing the VCO's out-of-band phase noise with the system bandwidth requires a sinusoidal signal at the desired offset. This waveform then reflects the VCO's noise spectrum around the offset, putting it back into the band. When we integrate the noise power (which must be 114 dB/Hz below the carrier at a 1-MHz offset), over the band of interest, this noise power has to be far stronger than the thermal noise so that we can measure it.

The channel filter suppresses the fundamental signal by 16.8 dB, so we can set the fine VGA gain to its maximum (typically 16 dB), yielding a 43-dB path gain. The integrated VCO phase noise level is then 6.3 mV. Although this signal power is adequately above the thermal-noise level, the quantization noise from a 5-bit ADC once again poses a significant signal observability problem.

In these calculations, we assume that the PLL bandwidth is less than the VCO measurements offset, making the VCO the dominant spectrum contributor. Thus, a wide-bandwidth  $\Sigma$ - $\Delta$  loop is not desirable for isolating the in-band PLL and out-of-band VCO phase noise. Because the level of VCO phase noise is fairly small at large offsets from the transmitter's center frequency, we can extract the phase noise spectrum by measuring the phase noise at smaller offsets and interpolating with a  $1/f^2$  roll-off. When the transmitter uses a wide-loop filter, the PLL phase noise also interferes with this measurement, forcing the movement of the VCO measurement further away from the center frequency and lowering the test signal power. Thus, if the selected architecture uses a wider loop bandwidth, the testability problem is more severe.

#### In-band PLL phase noise

The major contributor to the in-band phase noise is the PLL phase noise. Once again, because the input requires a simple sinusoidal waveform, and the output requires spectral analysis, it is advantageous to conduct this test through the receiver path so that the output is at a lower frequency.

The in-band portion of the synthesizer noise generated by the PLL must be  $-85$  dB below the carrier. To emphasize the PLL phase noise's effect, the fundamental signal must be at its maximum so that the resultant in-band phase noise is well above the thermal-noise floor. Applying a  $-20$ -dBm sinusoidal input at the carrier frequency minimizes path gain (19 dB); the major contributor to the total noise level is then the integrated phase noise of 11.2 mV at the input ADC.

#### Third-order intercept

Although engineers typically test  $IIP_3$  on a per-block basis, it is a system-level specification directly testable as a pinout parameter. Because  $IIP_3$  essentially specifies the system's linearity requirements, testing it requires a two-tone signal. To obtain easily observable signals, the input power level must be as high as possible. However, to avoid saturation, the power level of both fundamental signals must be 6 dB below the full signal range.

Because the  $IIP_3$  parameter is a hypothetical point, we must interpolate it from the measured data, as Figure 5 shows. Given the  $IIP_3$  requirement and the input power, we can estimate the harmonic power as

$$IIP_3 + G - H_3 = 3(IIP_3 - H_{1in})$$

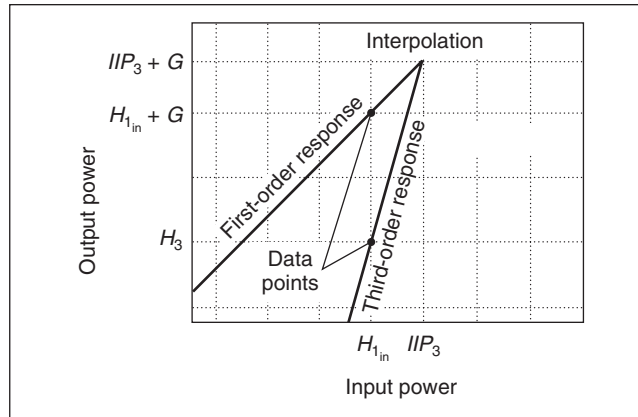
$$H_3 = G + 3H_{1in} - 2IIP_3$$

The path gain before the channel filter is 1.5 dB for the given signal amplitude. Assuming the channel filter suppresses the two fundamental signals, the gain after this point will be 25 dB. We derived the  $IIP_3$  specification to be greater than -20 dBm. With these specifications, the test signal for measurement at the ADC input is -11.5 dBm. Although a better linearity than the specified value implies a lower harmonic level, guaranteeing that we can observe this signal level also guarantees full fault coverage of the  $IIP_3$  parameter.

#### Frequency accuracy and drift

The VCO's absolute frequency can vary within a certain tolerance. Furthermore, it may drift in time with a limit of 400 Hz/ $\mu$ s.<sup>1</sup> Frequency drift is particularly a problem with the open-loop transmitter configuration.

To test for the absolute frequency accuracy, we can apply a fixed-frequency signal to the receiver path. Next, we open the loop, even though the normal mode might be to operate the synthesizer in a closed loop on the receiver path to cope with frequency drift during acquisition searches. We can then observe the frequency



**Figure 5. Interpolation of  $IIP_3$ .** With the input-output graph plotted in the log domain, the first-order response has a slope of 1, and the third-order response has a slope of 3. The measured fundamental and third-order harmonic levels provide the required data points to interpolate both responses.  $IIP_3$  is then the input point where the two response lines intersect.

drift at the base band. Because there are no other components that would induce fluctuations into the output signal's frequency, we can easily conduct this test in the integrated environment.

Table 3 shows a summary of the test requirements for the specifications we considered.

#### Hardware implications

To prevent costly iterations and last-minute test-point insertions into the system, engineers should conduct testability analysis and consider test issues during system design. Cost-effective solutions require analyzing testability in terms of test applicability and design considerations to simplify testing.

**Table 3. Summary of test requirements.**

Specification	Input	Expected signal at output	Measured quantity or characteristic
Filtering	-20 dBm, single tone	16 mV (minimum)	Spectrum
VCO phase noise	-20 dBm, single tone	6.3 mV	Noise
PLL phase noise	-20 dBm, single tone	11.2 mV	Noise
$IIP_3$	-26 dBm, two tone	71 mV	Spectrum
RMS phase noise	Digital	Modulated carrier	Down-conversion demodulation constellation
Spur level	Digital	85 mV	Spectrum
Frequency error	-20 dBm, single tone	188 mV	Frequency
Frequency drift	Digital	0 dBm	Spectrum

For Bluetooth specifications, out-of-band VCO phase noise and filtering characteristics at 2 MHz and above cause small signal amplitudes (the 6.3 mV in Table 3) that can fall below the quantization noise floor, depending on the ADC resolution.

We obtained these results with respect to an example system designed to minimally meet the specifications. Even though such a system could be the most cost-effective choice from a design perspective, the inherent testability problems increase the overall production cost. So we address possible changes in the system design that would eliminate these testability problems.

Increasing the observability of the test signals for the filtering and out-of-band phase noise tests requires increasing either the output signals' power or the ADC's resolution. There are two possible ways to increase the output signal levels:

- Design the system to accommodate signal levels larger than the specified maximum.
- During test mode, increase the gain of the fine VGA.

Unless the system is designed with a certain margin in terms of maximum input signal power, applying signals larger than  $-20$  dBm can cause compression at the mixer and high harmonic levels that can pollute the signal spectrum with the current mixer specifications. Therefore, increasing the maximum signal level means increased linearity specifications for the mixer, thereby consuming more power. Increasing the fine VGA's gain during test mode could be a lower-cost solution.

Increasing the ADC's resolution can reduce the quantization noise level. Clearly, such a modification has power and die-size implications as well. The lowest-cost solution depends on the flexibility of the implemented system and perhaps lies in increasing both the input power level and the resolution such that the power consumption and the die size do not increase significantly.

Furthermore, it is advantageous to decouple the receiver and transmitter loop oscillations. Such decoupling lets an external source drive

the receiver, whereas the internal synthesizer operates in the transmitter section. Thus, engineers can use the receiver to test and measure the transmitter signal. Finally, to detect defective parts during wafer sort, it is advantageous to choose an architecture that will allow loop-back test at the die level.

**THIS CASE STUDY** proposes that by integrating testability considerations into the design flow of radio transceivers, both at the architectural and block design levels, it's possible to outline low-cost test solutions. In future work, we plan to investigate various implemented Bluetooth designs for test cost, and incorporate DFT solutions and path-based test approaches. ■

## Acknowledgments

This work is partially supported through an IBM fellowship, the National Semiconductor Corp., and the University of California Micro Office.

## References

1. *Bluetooth Wireless Specification*, Bluetooth Special Interest Group, 1999; <http://www.Bluetooth.com/dev/specifications.asp>.
2. M.S. Heutmaker and D.K. Le, "An Architecture for Self-Test of a Wireless Communication System Using Sampled IQ Modulation and Boundary Scan," *IEEE Comm.*, vol. 37, no. 6, June 1999, pp. 98-102.
3. M. Jarwala, L. Duy, and M.S. Heutmaker, "End-to-End Test Strategy for Wireless Systems," *Proc. Int'l Test Conf. (ITC 95)*, IEEE Press, Piscataway, N.J., 1995, pp. 940-946.
4. R.G. Meyer, W.D. Mack, and J.E.M. Hageraats, "A 2.5-GHz BiCMOS Transceiver for Wireless LAN," *Proc. Int'l Solid-State Circuits Conf. (ISSCC 97)*, *Digest of Technical Papers*, IEEE Press, Piscataway, N.J., 1997, pp. 310-311.
5. B. Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LANs," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, Oct. 1999, pp. 1382-1385.
6. D.E. Fague et al., "Performance Evaluation of a Low Cost, Solid State Radio Front End for DECT," *Proc. 44th IEEE Vehicular Technology Conf. (VTC 94)*, IEEE Press, Piscataway, N.J., 1994, pp. 512-515.



**Sule Ozev** is a PhD student in the Computer Engineering Department at the University of California at San Diego. Her research interests include mixed-signal test, high-level test approaches, and test-access mechanisms for systems on chips. Ozev has a BS in electrical and electronics engineering from Bogazici University, Turkey, and an MS in computer engineering from the University of California at San Diego.



**Christian V. Olgaard** is cofounder and vice president of engineering at LitePoint. His research interests include wireless transceiver architecture design, RF CMOS circuit design, and cost-optimized wireless system and test solutions. Olgaard has an MS and PhD in electrical engineering from the Technical University of Denmark.



**Alex Orailoglu** is a professor of computer science and engineering at the University of California at San Diego. His research interests include digital and analog test, fault-tolerant computing, CAD, and embedded processors. Orailoglu has an SB in applied mathematics from Harvard University and an MS and PhD in computer science from the University of Illinois at Urbana-Champaign. He is a member of the IEEE Test Technology Technical Council executive committee, TTTC vice chair, and a Golden Core member of the IEEE Computer Society.

■ Direct questions and comments about this article to Sule Ozev, CSE Dept., Univ. of California at San Diego, La Jolla, CA 92093; sozev@cs.ucsd.edu.

**For further information on this or any other computing topic, visit our Digital Library at <http://computer.org/publications/dlib>.**

## Panel Announcement

### “Test as an Enabler for and Contributor to Faster Yield Ramp-up”

Look for a Panel Summary in a future issue of *IEEE Design & Test* on this panel (coorganized by VTS 2002 and *IEEE D&T*), held on 29 April 2002 at the 20th IEEE VLSI Test Symposium (28 April-2 May 2002, Monterey, Calif.).

The panel organizer is R. Segers (Philips Research). The moderator is J. Segal (HPL Technologies). Panelists include

- R. Aitken (Agilent),
- S. Eichenberger (Philips),
- A. Gattiker (IBM),
- M. Mollegan (HPL Technologies), and
- S. Venkataraman (Intel).

**For more information on VTS, see <http://www.tttc-vts.org/>.**

IEEE  
**Design&Test**  
of Computers