Class Review and Sample Exam Questions

CSE 237A

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Class Overview

• Plan for today:
  – Class review and sample questions from previous exams

• Upcoming:
  – HW3 due today
  – Exam the last day of class; no book/notes
    • Bring one 8 ½ x 11” sheet of paper with handwritten notes

• Course evaluations are out!!!!
  – Please provide your feedback re. course – we take your feedback very seriously & look forward to hearing from you!
Course Objectives

• Develop an understanding of the technologies behind the embedded computing systems
  – technology capabilities and limitations of the hardware, software components
  – methods to evaluate design tradeoffs between different technology choices.
  – design methodologies

• Overview of a few exciting research topics in embedded systems
Topics covered

• Embedded development platforms
  – ARM, RPi, Android, Arduino
• CPUs, GPUs, DSPs, FPGAs
• Memory
  – Caching, scratch pad, ARM mem. hierarchy, NVMs
• Interfacing w peripherals
  – Pooling, interrupts, DMA, GPIO, I2C, serial protocols
• AD/DA conversion
  – Nyquist theorem, aliasing, quantization
• Sensors, actuators (e.g. motors, servos, stepper motors, PWM)
• Timing & real-time scheduling
  – Clock synchronization, logical clocks
  – Independent processes: EDF, RM etc.; Dependent processes: ASAP, ALAP, List scheduler
  – Priority inversion and inheritance
• Real-time operating systems & Middleware
  – VxWorks, FreeRTOS, RT-Linux; PALOS, TinyOS; uCOS-II, eCOS
• Real-time IO
  – Profibus, CAN, ARINC, TTP/A & C, FlexRay; wireless
• HW/SW codesign
• Models of Computation
  – StateCharts, SDL, PetriNets, data flow, SDFs, Esterel, Verilog/VHDL, UML
Logical clocks

- What are the scalar and vector time representation of point $x$?
Real-time Schedulers

<table>
<thead>
<tr>
<th>Task</th>
<th>WCET</th>
<th>Period=Deadline</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>C</td>
<td>2</td>
<td>unknown</td>
</tr>
</tbody>
</table>

Min period of C for RM schedule = 8
Dependent Task Scheduling

- Add/Sub = 1 cycle  Mul = 2 cycles;
- Assume there are 2 multipliers, one adder
- Design a list schedule using mobility as a task priority metric

\[ O_1 := i_1 * i_2 + i_3 * i_4 \]
\[ O_2 := O_1 + i_5 \]
\[ O_3 := i_6 + i_7 \]
\[ O_4 := O_3 * i_8 \]
\[ O_5 := O_2 + O_4 \]
StateChart Problem
Exam Review: Petri Net

• **Initial marking:** \([1\ 0\ 0\ 0]\)
SDF

Diagram of nodes A, B, and C with labeled edges:
- A to B: 2
- A to C: 3
- B to A: 6
- B to C: 8
- C to B: 4
- C to A: 4
- B to D: 2
- C to D: 3
- D to B: 6
- D to C: 8

Nodes A, B, and C are connected in a triangular network.
Resources and SDF

• Find the fastest and lowest energy schedule assuming SDF tasks have to be executed sequentially, on following HW:

<table>
<thead>
<tr>
<th></th>
<th>Sensor node</th>
<th>DSP</th>
<th>CPU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execution times (seconds)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Task A</td>
<td>1</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td>Task B</td>
<td>-</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>Task C</td>
<td>-</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>Power consumption</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static power</td>
<td>1W</td>
<td>3W</td>
<td>5W</td>
</tr>
<tr>
<td>Dynamic power</td>
<td>1W</td>
<td>1W</td>
<td>20W</td>
</tr>
</tbody>
</table>
Module Test
Input A, B, C, D, F, H;
Output E, G, O;

abort
  loop
    await B || await C
    present D emit E else
    abort
    await F; emit G;
    when H
  end
when A do
  emit O;
end module;