CSE140: Components and Design Techniques for Digital Systems

Midterm #2 Sample Problems

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Where we are now…

• What we have covered:
  – Combinational and sequential circuits

• What we’ll do today:
  – Midterm review

• Deadlines:
  – HW due today, solutions posted tomorrow at class time
  – Midterm #2 this Wednesday
    • All material up to and including today
    • Bring one 8 ½ x 11” paper with handwritten notes
    • ID, pencil and eraser
Minimum POS of Decoder-Mux Circuit

This design has:

A. 2 inputs & 1 output

B. 4 inputs & 1 output

C. 2 states; output is Moore

D. B. & C.

E. None of the above

\[ f = (A + B + C + D) \]
\[ (A + B + C + D) \]
\[ (A + B + C + D) \]

Sources: TSR, Katz, Boriello, Vahid, Perkowski
What does this circuit do?

Is this circuit:
A. Latch
B. Flip-flop
C. None of the above
What does this circuit do?

The following is true for the circuit on the left:

A. Moore outputs
B. It has one input
C. All of the above
D. None of the above

\[ t_{ccq} + t_{cd} > t_{hold} + t_{skew} \]
\[ T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew} \]
\[ 2 \text{ps} \]
\[ 1 + 2 > 2 \]
\[ f = \frac{1}{15 \text{ps}} \]
What does this circuit do?

Assume that both D-FFs are reset at start.

The following is true for the circuit on the left:
A. It is Mealy FSM
B. It has a mux
C. It has one input
D. It uses a decoder
E. None of the above

Sources: TSR, Katz, Boriello, Vahid, Perkowski
FSM design: Multiple input counter

- Given FSM of a multiple input counter, design the circuit implementing its functionality

<table>
<thead>
<tr>
<th>present state</th>
<th>next state</th>
<th>output</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>S0 S1 S2 S3</td>
<td>1</td>
</tr>
<tr>
<td>S1</td>
<td>S0 S3 S1 S3</td>
<td>0</td>
</tr>
<tr>
<td>S3</td>
<td>S1 S0 S0 S3</td>
<td>0</td>
</tr>
<tr>
<td>S2</td>
<td>S1 S3 S2 S0</td>
<td>1</td>
</tr>
</tbody>
</table>

The following is true for this design:

A. It has one output that is Mealy  
B. It has two states  
C. It has no inputs
D. None of the above
Multiple input counter: Logic for D-FF

- Derive logic equations for inputs of D-FF

<table>
<thead>
<tr>
<th>Input</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>00</td>
<td>01</td>
<td>01</td>
</tr>
<tr>
<td>01</td>
<td>01</td>
<td>11</td>
<td>00</td>
<td>11</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>11</td>
<td>11</td>
<td>00</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>01</td>
<td>00</td>
<td>10</td>
</tr>
</tbody>
</table>

\[ D_0 = (Q_1 + I_1 + I_0) \]
\[ D_1 = \left( \left( Q_1 + I_1 + I_0 \right) \right) \]

Sources: TSR, Katz, Boriello, Vahid, Perkowski
Logic & Timing diagrams
FSM design example

• Design an overlapping finite string pattern recognizer
  – output is 1 whenever the input sequences 101 and 011 are observed
ALU design

- Design at 2 bit ALU using the specification given below with maximum two full adders and minimum number of other elements.

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_0$</th>
<th>ALU Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$F_i = (A_i == B_i)$ (bitwise equality)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$F_i = (A_i &lt; B_i)$ (bitwise strictly less than)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$F_i = A_i + B_i + 1$ (addition, then increment)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$F_i = A_i - B_i - 1$ (subtraction, then decrement)</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello, Vahid, Perkowski