Midterm 1 Results

Average: 84.7
Median: 86.5
Standard Deviation: 16.3
Max: 108
Min: 37

Sources: TSR, Katz, Boriello & Vahid
Arithmetic Logic Unit – Example 2

If \( F_2 = 0 \) then:

A) Left

B) Right

<table>
<thead>
<tr>
<th>( F_{2:0} )</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>A &amp; B</td>
</tr>
<tr>
<td>001</td>
<td>A</td>
</tr>
<tr>
<td>010</td>
<td>A + B</td>
</tr>
<tr>
<td>011</td>
<td>Not used</td>
</tr>
<tr>
<td>100</td>
<td>A &amp; ~B</td>
</tr>
<tr>
<td>101</td>
<td>A</td>
</tr>
<tr>
<td>110</td>
<td>A - B</td>
</tr>
<tr>
<td>111</td>
<td>Not used</td>
</tr>
</tbody>
</table>
CSE140: Components and Design Techniques for Digital Systems

Sequential Circuit Introduction
Latches and Flip-Flops

Tajana Simunic Rosing
What is a sequential circuit?

A circuit whose output depends on current inputs and past outputs

A circuit with memory

\[ y_i = f_i(S^t, X) \]
\[ s_{i+1} = g_i(S^t, X) \]
Why do we need circuits with ‘memory’?

- Circuits with memory can be used to store data
- Systems have circuits that run a sequence of tasks

**Memory Hierarchy**

- Registers
- Cache
- Main Memory
- Hard disk

Sources: TSR, Katz, Boriello & Vahid
Simplest memory element

SRAM (Static Random Access Memory)

"data"

"load"

"remember"

"stored value"
Flight attendant call button

- Flight attendant call button
  - Press call: light turns on
    - *Stays on* after button released
  - Press cancel: light turns off
  - Logic circuit to implement this?

- SR latch implementation
  - Call=1 : sets Q to 1 and keeps it at 1
  - Cancel=1 : resets Q to 0

Sources: TSR, Katz, Boriello & Vahid
SR Latch Analysis

- $S = 1, R = 0$:
  then $Q = 1$ and $\overline{Q} = 0$

- $S = 0, R = 1$:
  then $\overline{Q} = 1$ and $Q = 0$

Sources: TSR, Katz, Boriello & Vahid
SR Latch Analysis

- $S = 0$, $R = 0$:
  
  then $Q = Q_{prev}$

  - Memory!

- $S = 1$, $R = 1$:
  
  then $Q = 0$, $\bar{Q} = 0$

  - Invalid State

  $\bar{Q} \neq \text{NOT } Q$
What if a kid presses both call and cancel & then releases them?

- If $S=1$ and $R=1$ at the same time and then released, $Q =$?
  - Can also occur also due to different delays of different paths
  - $Q$ may oscillate and eventually settle to 1 or 0 due to diff. path delay

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>hold</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>not allowed</td>
</tr>
</tbody>
</table>
SR Latch Symbol

• SR stands for Set/Reset Latch
  – Stores one bit of state ($Q$)

• Control what value is being stored with $S$, $R$ inputs
  – **Set:** Make the output 1
    $$(S = 1, \ R = 0, \ Q = 1)$$
  – **Reset:** Make the output 0
    $$(S = 0, \ R = 1, \ Q = 0)$$
  – **Hold:** Keep data stored
    $$(S = 0, \ R = 0, \ Q = Q_{\text{previous}})$$
SR Latch Characteristic Equation

To analyze, break the feedback path

\[
Q(t+\Delta) = S + R' Q(t)
\]

State Diagram

Sources: TSR, Katz, Boriello & Vahid
Avoiding $S=R=1$ Part 1: Level-Sensitive SR Latch

- Add input “C”
  - Change C to 1 only after S and R are stable
  - C is usually a clock (CLK)
Clocks

- **Clock** -- Pulsing signal for enabling latches; ticks like a clock
- **Synchronous** circuit: sequential circuit with a clock

- **Clock period**: time between pulse starts
  - Above signal: period = 20 ns
- **Clock cycle**: one such time interval
  - Above signal shows 3.5 clock cycles
- **Clock duty cycle**: time clock is high
  - 50% in this case
- **Clock frequency**: 1/period
  - Above: freq = 1 / 20ns = 50MHz;

<table>
<thead>
<tr>
<th>Freq</th>
<th>Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 GHz</td>
<td>0.01 ns</td>
</tr>
<tr>
<td>10 GHz</td>
<td>0.1 ns</td>
</tr>
<tr>
<td>1 GHz</td>
<td>1 ns</td>
</tr>
<tr>
<td>100 MHz</td>
<td>10 ns</td>
</tr>
<tr>
<td>10 MHz</td>
<td>100 ns</td>
</tr>
</tbody>
</table>
Clock question

The clock shown in the waveform below has:

A. Clock period of 4ns with 250MHz frequency
B. Clock duty cycle 75%
C. Clock period of 1ns with 1GHz frequency
D. A. & B.
E. None of the above

A. Clock period of 4ns with 250MHz frequency ✓
B. Clock duty cycle 75% ✓
C. Clock period of 1ns with 1GHz frequency
D. A. & B.
E. None of the above
CSE140: Components and Design Techniques for Digital Systems

Latches and Flip-Flops

Tajana Simunic Rosing
Where we are….

• Last time:
  – Memory, SR latch

• Plan for today:
  – Latches and flip flops

• Deadlines coming up:
  – HW assigned, due Monday at the beginning of the class
    • 4 problems, 2 graded
  – Zybook due at the beginning of the class

• Reminders
  – Discussion session on Friday

Sources: TSR, Katz, Boriello & Vahid
Avoiding $S=R=1$ Part 2: Level-Sensitive D Latch

- SR latch requires careful design so $SR=11$ never occurs
- D latch helps by inserting the inverter between $S$ & $R$ inputs
  - Inserted inverter ensures $R$ is always the opposite of $S$ when $C=1$

Sources: TSR, Katz, Boriello & Vahid
D Latch Truth Table

<table>
<thead>
<tr>
<th>CLK</th>
<th>D</th>
<th>\overline{D}</th>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>\overline{Q}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>prev</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello & Vahid
D Latch Summary

- Two inputs: $CLK$, $D$
  - $CLK$: controls *when* the output changes
  - $D$ (the data input): controls *what* the output changes to

- Function
  - When $CLK = 1$, $D$ passes through to $Q$ (*transparent*)
  - When $CLK = 0$, $Q$ holds its previous value (*opaque*)

- (Mostly) avoids invalid case $Q = \overline{Q}$

Sources: TSR, Katz, Boriello & Vahid
Assume that data in all latches is initially 0. Input $Y=1$ and $Clk$ transitions from 0-$\rightarrow$1. When $Clk=0$ again, the stored values in latches are:

A. $Q1=1$, $Q2=0$, $Q3=0$, $Q4=0$ for both clock A & B
B. $Q1=1$, $Q2=1$, $Q3=1$, $Q4=1$ for clock A
C. $Q1=1$, $Q2=0$, $Q3=0$, $Q4=0$ for clock B
D. More information is needed to determine the answer
E. None of the above
• **Flip-flop**: Bit storage that stores on the clock edge, not level
• Master-slave design: master loads when Clk=0, then slave when Clk=1
D Flip-Flop: Characteristic Equation

Characteristic Equation

\[ Q(t+1) = D(t) \]

<table>
<thead>
<tr>
<th>Id</th>
<th>D</th>
<th>Q(t)</th>
<th>Q(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello & Vahid
Bit Storage Overview

**SR latch**

- S (set)
- R (reset)

S=1 sets Q to 1, R=1 resets Q to 0.

Problem: SR=11 yield undefined Q.

**Level-sensitive SR latch**

- S
- C
- R

S and R only have effect when C=1. We can design outside circuit so SR=11 never happens when C=1.

Problem: avoiding SR=11 can be a burden.

**D latch**

- D
- C

SR can’t be 11 if D is stable before and while C=1, and will be 11 for only a brief glitch even if D changes while C=1.

Problem: C=1 too long propagates new values through too many latches: too short may not enable a store.

**D flip-flop**

- D
- Clk

Only loads D value present at rising clock edge, so values can’t propagate to other flip-flops during same clock cycle.

Tradeoff: uses more gates internally than D latch, and requires more external gates than SR – but gate count is less of an issue today.
CSE140: Components and Design Techniques for Digital Systems

Latches, Flip-Flops

Registers & Counters

Tajana Simunic Rosing
Bit Storage Overview

**SR latch**
- S (set) and R (reset)
- S=1 sets Q to 1, R=1 resets Q to 0.
- Problem: SR=11 yield undefined Q.

**Level-sensitive SR latch**
- S and R only have effect when C=1.
- Problem: avoiding SR=11 can be a burden.

**D latch**
- SR can’t be 11 if D is stable before and while C=1, and will be 11 for only a brief glitch even if D changes while C=1.
- Problem: C=1 too long propagates new values through too many latches: too short may not enable a store.

**D flip-flop**
- Only loads D value present at rising clock edge, so values can’t propagate to other flip-flops during same clock cycle.
- Tradeoff: uses more gates internally than D latch, and requires more external gates than SR – but gate count is less of an issue today.

**SRAM cell has**
- A) 6 transitions
- 4 trans

**B)** \( \text{Rin} + 2 \text{ trans} \)
- \( \times 2 \text{ gobs} \)
- \( \in \) A & B

Sources: TSR, Katz, Boriello & Vahid
Rising vs. Falling Edge D Flip-Flop

The triangle means clock input, edge triggered

Symbol for rising-edge triggered D flip-flop

Internal design: Just invert servant clock rather than master

Symbol for falling-edge triggered D flip-flop

rising edges

Clk

falling edges

Clk

Sources: TSR, Katz, Boriello & Vahid
Enabled D-FFs

- **Inputs:** \(CLK, D, EN\)
  - The enable input \((EN)\) controls when new data \((D)\) is stored.

- **Function**
  - \(EN = 1\): \(D\) passes through to \(Q\) on the clock edge.
  - \(EN = 0\): the flip-flop retains its previous state.

Sources: TSR, Katz, Boriello & Vahid
Additional D-FF Features

- Reset (set state to 0) – R
  - synchronous: \(D_{\text{new}} = R' \cdot D_{\text{old}}\) (when next clock edge arrives)
  - asynchronous: doesn’t wait for clock

- Preset or set (set state to 1) – S (or sometimes P)
  - synchronous: \(D_{\text{new}} = D_{\text{old}} + S\) (when next clock edge arrives)
  - asynchronous: doesn’t wait for clock

- Both reset and preset
  - \(D_{\text{new}} = R' \cdot D_{\text{old}} + S\) (set-dominant)
  - \(D_{\text{new}} = R' \cdot D_{\text{old}} + R'S\) (reset-dominant)

- Selective input capability (input enable or load) – LD or EN
  - multiplexor at input: \(D_{\text{new}} = LD' \cdot Q + LD \cdot D_{\text{old}}\)
  - lead may or may not override reset/set (usually R/S have priority)

- Complementary outputs – Q and Q'
Comparison of latches and flip-flops

- **positive edge-triggered flip-flop**
- **level-sensitive latch**

Sources: TSR, Katz, Boriello & Vahid
D Flip-Flops

Assume that the data in all D-FFs is initially 0. Input Y=1. When Clk goes from 0->1, the stored values in D-FFs are:

A. Q1=1, Q2=0, Q3=0, Q4=0 for both clock A & B
B. Q1=1, Q2=1, Q3=1, Q4=1 for clock A
   Q1=1, Q2=0, Q3=0, Q4=0 for clock B
C. Q1=1, Q2=1, Q3=1, Q4=1 for both clocks
D. More information is needed to determine the answer
E. None of the above
Registers and Counters
Building blocks with FFs: Basic Register

D Q
CLK
IN1
OUT1
D Q
IN2
OUT2
D Q
IN3
OUT3
D Q
IN4
OUT4
Q3 Q2 Q1 Q0
reg(4)

Sources: TSR, Katz, Boriello & Vahid
Shift register

- Holds & shifts samples of input
Pattern Recognizer

- Combinational function of input samples

Sources: TSR, Katz, Boriello & Vahid
Design of a Universal Shift Register

Nth cell

<table>
<thead>
<tr>
<th>clear</th>
<th>s0</th>
<th>s1</th>
<th>new value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Output value of FF to left (shift right)
Output value of FF to right (shift left)

Input

Sources: TSR, Katz, Boriello & Vahid
Counters

• Sequences through a fixed set of patterns

\[\text{LFSR}\]
General Counters

- Default operation: count up
  - QA-QD counter output
  - A-D parallel load data
  - LOAD enables data load
  - RCO ripple carry out
  - CLR clears data
  - EN counter enable

Sources: TSR, Katz, Boriello & Vahid
Finite State Machines
Circuit Specifications

- **Combinational Logic**
  - Truth tables, Boolean equations, logic diagrams (no feedback)

- **Sequential Networks**: State Diagram (Memory)
  - State and Excitation Tables
  - Characteristic Expression
  - Logic Diagram (FFs and feedback loops)

RTL: Register-Transfer Level Description
Finite State Machines: Two Bit Counter Example

Symbol/ Circuit

State Diagram

2 bit Counter

Current state | Next State
---|---
S₀ | S₁
S₁ | S₂
S₂ | S₃
S₃ | S₀

State Table

<table>
<thead>
<tr>
<th>Q₁(t)</th>
<th>Q₀(t)</th>
<th>Q₁(t+1)</th>
<th>Q₀(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Which is the most likely circuit realization of the two bit counter?

**State Table**

<table>
<thead>
<tr>
<th>$Q_1(t)$</th>
<th>$Q_0(t)$</th>
<th>$Q_1(t+1)$</th>
<th>$Q_0(t+1)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

A. **Combinational circuit**

B. **Combinational circuit**

C. **Combinational circuit**

D. **Circuit with no flip flops**

E. **Circuit with 2 flip flops**

F. **Circuit with one flip flop**

Sources: TSR, Katz, Boriello & Vahid
Finite State Machines
Where we are….

• Last time:
  – Memory, latches, flip flops, registers, counters

• Plan for today:
  – FSM

• Deadlines coming up:
  – HW assigned, due Monday at the beginning of the class
    • 4 problems, 2 graded
  – Zybook due at the beginning of the class

• Reminders
  – Discussion session on Friday

Sources: TSR, Katz, Boriello & Vahid
Combinational vs. Sequential

- **Combinational Logic**
  - Truth tables, Boolean equations, logic diagrams (no feedback)

- **Sequential Networks: FSMs**
  - State and Excitation Tables
  - Characteristic Expression
  - Logic Diagram (FFs and feedback loops)

RTL: Register-Transfer Level Description

Sources: TSR, Katz, Boriello & Vahid
Finite State Machine (FSM) Definition

- FSM consists of
  - Set of states
  - Set of inputs, set of outputs
  - Initial state
  - Set of transitions
    - Only one can be true at a time

- FSM representations:
  - State diagram
  - State table
FSM Example

Watch for transition properties!
(note that more transitions need to be added)

Inputs: s,r,g,b,a;
Outputs: u

Is this FSM fully defined?
A. Yes
B. No

Sources: TSR, Katz, Boriello & Vahid
We store the current state using D-flip flops so that:

- Inputs to the combinational circuit don’t change while the next output is computed
- The transition to the next state only occurs at the rising edge of the clock

\[
D_0(t) = Q_0(t)'
\]
\[
D_1(t) = Q_0(t) Q_1(t)' + Q_0(t)' Q_1(t)
\]
FSM Controller Design Process with a Three Bit Counter Example

1. State Diagram
2. State Table
3. State Assignments
4. Excitation Table
   (present state, inputs; next state, outputs)
5. Circuit

Excitation Table with Assigned State Patterns

<table>
<thead>
<tr>
<th>C3</th>
<th>C2</th>
<th>C1</th>
<th>N3</th>
<th>N2</th>
<th>N1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>1</td>
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<td>1</td>
<td>1</td>
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<tr>
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<td>1</td>
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</tr>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello & Vahid
Mealy and Moore Machines

Mealy Machine: \( y_i(t) = f_i(X(t), S(t)) \)
Moore Machine: \( y_i(t) = f_i(S(t)) \)

\[ s_i(t+1) = g_i(X(t), S(t)) \]
This Counter Design Is:
A. Moore machine
B. Mealy machine
C. None of the above
This pattern recognizer should have
A. One state because it has one output
B. One state because it has one input
C. Two states because the input can be 0 or 1
D. More than two states because ….
E. None of the above
Which of the following diagrams is a correct Mealy solution for the 001 pattern recognizer on the Mars rover?

A.  

B.  

C. Both A and B are correct  

D. None of the above
What does state table need to show to design controls of C1?
A. (current input $x(t)$, current state $S(t)$ vs. next state, $S(t+1)$)
B. (current input, current state vs. current output $y(t)$)
C. (current input, current state vs. current output, next state)
D. None of the above
State Diagram => State Table with State Assignment

State Assignment

<table>
<thead>
<tr>
<th>S(t) \ x</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>S1,0</td>
<td>S0,0</td>
</tr>
<tr>
<td>S1</td>
<td>S2,0</td>
<td>S0,0</td>
</tr>
<tr>
<td>S2</td>
<td>S2,0</td>
<td>S0,1</td>
</tr>
</tbody>
</table>

Mealy Machine

\[ S(t) = \begin{array}{c}
1/0 \\
0/0 \\
0/0 \\
1/0
\end{array} \]

\[ x(t) = \begin{array}{c}
1/1 \\
0/0
\end{array} \]

\[ C1 \rightarrow C2 \]

\[ y(t) = \begin{array}{c}
0/0 \\
1/0
\end{array} \]

\[ Q_1(t+1)Q_0(t+1), y \]

Sources: TSR, Katz, Boriello & Vahid
State Diagram $\Rightarrow$ State Table $\Rightarrow$ Excitation Table $\Rightarrow$ Circuit

<table>
<thead>
<tr>
<th>$Q_1(t)$</th>
<th>$Q_0(t)$</th>
<th>$x$</th>
<th>$Q_1(t)$</th>
<th>$Q_0(t)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>01,0</td>
<td>01</td>
<td>00</td>
<td>00,0</td>
</tr>
<tr>
<td>01</td>
<td>10,0</td>
<td>10</td>
<td>00</td>
<td>00,0</td>
</tr>
<tr>
<td>10</td>
<td>10,0</td>
<td>10</td>
<td>00</td>
<td>00,1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>id</th>
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Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table => Excitation Table => Circuit

### State Table

<table>
<thead>
<tr>
<th>Q&lt;sub&gt;1&lt;/sub&gt;(t) Q&lt;sub&gt;0&lt;/sub&gt;(t)</th>
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<th>1</th>
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### Excitation Table

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<th>D&lt;sub&gt;1&lt;/sub&gt;</th>
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Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table => Excitation Table => Circuit

<table>
<thead>
<tr>
<th>id</th>
<th>Q₁Q₀x</th>
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D₁(t):

<table>
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<tr>
<th>Q₀</th>
<th>Q₁</th>
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<tbody>
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</table>

D₁(t) = x’Q₀ + x’Q₁
D₀(t) = Q’₁Q’₀ x’

y = Q₁x

Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table => Excitation Table => Circuit

\[ D_1(t) = x'Q_0 + x'Q_1 \]
\[ D_0(t) = Q'_1Q'_0x' \]
\[ y = Q_1x \]
Moore FSM for the Mars Life Recognizer

Which of the following diagrams is a correct Moore solution to the ‘001’ pattern recognizer?

A. 1/0

B. 1/0 1

C. Both A and B are correct

D. None of the above
Moore Mars Life Recognizer: FF Input Specs

Pattern Recognizer ‘001’

Moore Machine

What does state table need to show to design controls of C2?
A. (current input x(t), current state S(t) vs. next state, S(t+1))
B. (current input, current state vs. current output y(t))
C. (current state vs. current output y(t) and next state)
D. (current state vs. current output y(t))
E. None of the above

Sources: TSR, Katz, Boriello & Vahid
Moore Mars Life Recognizer: State Table

### State Transition Diagram

- **States:** S0, S1, S2, S3
- **Input:** x
- **Output:** y

### State Table

<table>
<thead>
<tr>
<th>S(t) \ x</th>
<th>0</th>
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</thead>
<tbody>
<tr>
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<tr>
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### Input Table

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Sources: TSR, Katz, Boriello & Vahid
Mars Life Recognizer: Combinational Circuit Design

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<th>D1</th>
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Sources: TSR, Katz, Boriello & Vahid
Mars Life Recognizer Circuit Implementation

State Diagram => State Table => Excitation Table => Circuit

Moore Machine

Sources: TSR, Katz, Boriello & Vahid
15 cents for candy! Watch out – no change!

- **Moore machine**
  - outputs associated with state

- **Mealy machine**
  - outputs associated with transitions
Example: Moore implementation

- Encode states and map to logic

<table>
<thead>
<tr>
<th>present state</th>
<th>inputs</th>
<th>next state</th>
<th>output</th>
<th>open</th>
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open = Q1 Q0
Example: Mealy implementation

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<th>inputs</th>
<th>next state</th>
<th>output</th>
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</thead>
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</table>
Timing Constraints in Sequential Designs
Our seemingly logically correct design can go wrong – signals don’t travel in zero time 😞
We next look at timing constraints for combinational and sequential logic.
I. Min delay of a gate, also called contamination delay: $t_{cd}$
Minimum time from when an input changes until the output *starts* to change

II. Max delay of a gate, also called propagation delay: $t_{pd}$
Maximum time from when an input changes until the output *is* guaranteed to reach its final value (i.e., stop changing)
Which path in the above circuit determines the contamination delay of the circuit (assuming the delay of all the gates is the same)?

A. Blue path
B. Red path
C. Both
D. Neither
Which path in the above circuit determines the propagation delay of the circuit (assuming the delay of all the gates is the same)?

A. Blue path  
B. Red path  
C. Both  
D. Neither
D-FF Input Constraints: Setup and Hold Times

I. Setup time: $t_{\text{setup}}$
   Time before the clock edge that data must be stable (i.e. not change)

II. Hold time: $t_{\text{hold}}$
    Time after the clock edge that data must be stable

Aperture time: $t_a$
Time around clock edge that data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)

Sources: TSR, Katz, Boriello & Vahid
Output Timing Constraints

I. Min delay of FF, also called contamination delay or min CLK to Q delay: $t_{ccq}$
Time after clock edge that $Q$ might be unstable (i.e., starts changing)

II. Max delay of FF, also called propagation delay or maximum CLK to Q delay: $t_{pcq}$
Time after clock edge that the output $Q$ is guaranteed to be stable (i.e. stops changing)
The timing of which of the following signals can cause a setup-time violation?

A. The input signal D(t)  
B. The output signal Q(t)  
C. Both of the above 
D. None of the above
Causes of Timing Issues in Sequential Circuits

- Input to a FF comes from the output of another FF through a combinational circuit
- The FF and combinational circuit have a min & max delay

Which of the following violations occurs if max delay of R1 is zero & max delay of the combinational logic (CL) is equal to the clock period?

A. Hold time violation for R2
B. Setup violation for R2
C. Hold time violation for R1
D. Setup violation for R1
E. None of the above
Setup Time Constraint

- Input to a FF comes from the output of another FF through a combinational circuit
- The FF and combinational circuit have a min & max delay

\[ T_c \geq t_{\text{setup}} + \text{max delay(FF)} + \text{max delay(combinational)} \]

\[ f_c = \frac{1}{T_c} \]

Sources: TSR, Katz, Boriello & Vahid
Causes of Timing Issues in Sequential Circuits

- Input to a FF comes from the output of another FF through a combinational circuit
- The FF and combinational circuit have a min & max delay

Which of the violations would occur if the min delay of R1 was zero and the combinational circuit was just a wire?

A. Hold time violation for R2
B. Setup violation for R2
C. Hold time violation for R1
D. Setup violation for R1
E. None of the above
Hold Time Constraint

- Input to a FF comes from the output of another FF through a combinational circuit.
- The FF and combinational circuit have a min & max delay.

Hold Time Constraint:

\[ t_{\text{hold}} < \min \text{ delay(FF)} + \min \text{ delay(combinational)} \]

\[ t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}} \]
Once a flip flop has been built, its timing characteristics stay fixed: $t_{\text{setup}}$, $t_{\text{hold}}$, $t_{\text{ccq}}$, $t_{\text{pcq}}$.

What about the clock? Does the clock edge arrive at the same time to all the D-FFs on the chip?
Clock Skew

- The clock doesn’t arrive at all registers at the same time
- **Skew**: difference between the two clock edges
- Perform the **worst case analysis**
• In the worst case, CLK2 is earlier than CLK1
• $t_{pcq}$ is max delay through FF, $t_{pd}$ is max delay through logic

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew})$$
Hold Time Constraint with Skew

- In the worst case, CLK2 is later than CLK1
- \( t_{ccq} \) is min delay through FF, \( t_{cd} \) is min delay through logic

\[
\begin{align*}
    t_{ccq} + t_{cd} & > t_{\text{hold}} + t_{\text{skew}} \\
    t_{cd} & > t_{\text{hold}} + t_{\text{skew}} - t_{ccq}
\end{align*}
\]
Timing Analysis Example

Timing Characteristics

- $t_{ccq} = 30$ ps
- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps
- $t_{cd} = 25$ ps

Setup time constraint:

$T_c \geq (50 + 105 + 60)$ ps = 215 ps

$f_c = 1/T_c = 4.65$ GHz

Hold time constraint:

$t_{ccq} + t_{cd} > t_{hold}$?

$(30 + 25)$ ps $> 70$ ps? No!

Sources: TSR, Katz, Boriello & Vahid
Timing Analysis Example

Add buffers to the short paths:

Timing Characteristics

\[ t_{ccq} = 30 \text{ ps} \]
\[ t_{pcq} = 50 \text{ ps} \]
\[ t_{setup} = 60 \text{ ps} \]
\[ t_{hold} = 70 \text{ ps} \]
\[ t_{pd} = 35 \text{ ps} \]
\[ t_{cd} = 25 \text{ ps} \]

Setup time constraint:

\[ T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps} \]
\[ f_c = 1/T_c = 4.65 \text{ GHz} \]

Hold time constraint:

\[ t_{ccq} + t_{cd} > t_{hold} \]
\[ (30 + 50) \text{ ps} > 70 \text{ ps} \quad \text{Yes!} \]
Sequential Circuit Design Summary

- SRAM memory, SR Latch, D Latch, D-FF
- Design procedure for FSMs
  1. Capture FSM
  2. Create state table
  3. Assign the states
  4. Excitation table
  5. Implement the combinational logic
- Mealy vs. Moore FSM
- Non-ideal properties of FFs
  - Setup/hold time constraints
  - Maximum operating frequency
  - Clock skew
SEQUENTIAL DESIGN EXAMPLES

Prof. Tajana Simunic Rosing
CSE 140
Where we are….

• Last time:
  – Memory, latches, flip flops, registers, counters, FSMs & timing

• Plan for today:
  – Sequential circuit review

• Deadlines coming up:
  – HW assigned, due Monday at the beginning of the class
    • 4 problems, 2 graded
  – Zybook due at the beginning of the class

• Reminders
  – Discussion session
  – Exam #2 Feb 27th
    • 8 ½ x 11” sheet of paper with handwritten notes
    • Bring your ID, pencil and eraser
    • 4 problems, focus on recent material, but exam is cumulative
Sequential Circuit Design Summary

- SRAM memory, SR Latch, D Latch, D-FF
- Design procedure for FSMs
  1. Capture FSM
  2. Create state table
  3. Assign the states
  4. Excitation table
  5. Implement the combinational logic
- Mealy vs. Moore FSM
- Non-ideal properties of FFs
  - Setup/hold time constraints
  - Maximum operating frequency
  - Clock skew

Sources: TSR, Katz, Boriello & Vahid
What does this circuit do?

Options:
A) D-FF
B) D Latch
C) SR Latch
D) SRAM
E) No A

Q_{t+1} = Q_t \oplus X

Sources: TSR, Katz, Boriello & Vahid
What is the output of this circuit?

Do = Q2 ⊕ Q3

? circuit:
A) shift reg
B) random number gen
C) counter
D) all of above

Sources: TSR, Katz, Boriello & Vahid
FSM Design

<table>
<thead>
<tr>
<th>Q₁</th>
<th>Q₀</th>
<th>a</th>
<th>D₁</th>
<th>D₀</th>
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Input: a
Output: y

y = 0
y = 0
y = 1
y = 1

True
## FSM Analysis

<table>
<thead>
<tr>
<th>Q1Q0A</th>
<th>Q1(t+1)</th>
<th>Q0(t+1)</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
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</tbody>
</table>

The diagram on the right illustrates the state transitions and output logic for the FSM, with inputs A and A', and outputs Q0 and Y.