CSE140: Components and Design Techniques for Digital Systems

ALU, Latches and Flip-Flops

Tajana Simunic Rosing
Where we are….

• Last time:
  – ALUs

• Plan for today:
  – ALU example, latches and flip flops

• Exam #1 grades posted
  – Excellent work!!!
  – Regrade requests possible for 24hrs after grades are released
    • Submit request via gradescope
    • If not satisfied after the regrade, email me

• Deadlines coming up:
  – HW assigned, due Monday at the beginning of the class
    • 4 problems, 2 graded
  – Zybook due at the beginning of the class

• Reminders
  – Discussion session on Friday

Sources: TSR, Katz, Boriello & Vahid
Midterm 1 Results

Average: 84.7
Median: 86.5
Standard Deviation: 16.3
Max: 108
Min: 37

Sources: TSR, Katz, Boriello & Vahid
<table>
<thead>
<tr>
<th>Function</th>
<th>F2</th>
<th>F1</th>
<th>F0</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>A &amp; B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>001</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>A + B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>Not used</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>A &amp; ~B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>A - B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>Not used</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Arithmetic Logic Unit – Example 2**

**Sources:** TSR, Katz, Boriello & Vahid
CSE140: Components and Design Techniques for Digital Systems

Sequential Circuit Introduction
Latches and Flip-Flops

Tajana Simunic Rosing
What is a sequential circuit?

A circuit whose output depends on current inputs and past outputs

A circuit with **memory**

\[ y_i = f_i(S^t, X) \]
\[ s_{i+1} = g_i(S^t, X) \]
Why do we need circuits with ‘memory’?

- Circuits with memory can be used to store data
- Systems have circuits that run a sequence of tasks

Memory Hierarchy

- Registers
- Cache
- Main Memory
- Hard disk

Sources: TSR, Katz, Boriello & Vahid
Simplest memory element

SRAM

static

"data"

"load"

"remember"

"stored value"
Flight attendant call button

- Flight attendant call button
  - Press call: light turns on
    - *Stays on* after button released
  - Press cancel: light turns off
  - Logic circuit to implement this?

- SR latch implementation
  - Call=1: sets Q to 1 and keeps it at 1
  - Cancel=1: resets Q to 0

Sources: TSR, Katz, Boriello & Vahid
SR Latch Analysis

- $S = 1, R = 0$:
  then $Q = 1$ and $\overline{Q} = 0$

- $S = 0, R = 1$:
  then $Q = 1$ and $\overline{Q} = 0$
SR Latch Analysis

- \( S = 0, R = 0 \):
  
  then \( Q = Q_{\text{prev}} \)

  - Memory!

- \( S = 1, R = 1 \):
  
  then \( Q = 0, \overline{Q} = 0 \)

  - Invalid State

  \( Q \neq \text{NOT } Q \)

Sources: TSR, Katz, Boriello & Vahid
What if a kid presses both call and cancel & then releases them?

- If $S=1$ and $R=1$ at the same time and then released, $Q=？$
  - Can also occur also due to different delays of different paths
  - $Q$ may oscillate and eventually settle to 1 or 0 due to diff. path delay

Sources: TSR, Katz, Boriello & Vahid
SR Latch Symbol

• **SR** stands for Set/Reset Latch
  – Stores one bit of state ($Q$)

• Control what value is being stored with $S$, $R$ inputs
  – **Set**: Make the output 1
    $(S = 1, R = 0, Q = 1)$
  – **Reset**: Make the output 0
    $(S = 0, R = 1, Q = 0)$
  – **Hold**: Keep data stored
    $(S = 0, R = 0, Q = Q_{previous})$
SR Latch Characteristic Equation

To analyze, break the feedback path

\[
Q(t+\Delta) = S + R' Q(t)
\]

State Diagram

characteristic equation

Sources: TSR, Katz, Boriello & Vahid
Avoiding S=R=1 Part 1: Level-Sensitive SR Latch

- Add input “C”
  - Change C to 1 only after S and R are stable
  - C is usually a clock (CLK)
**Clocks**

- **Clock** -- Pulsing signal for enabling latches; ticks like a clock
- **Synchronous** circuit: sequential circuit with a clock

- **Clock period**: time between pulse starts
  - Above signal: period = 20 ns
- **Clock cycle**: one such time interval
  - Above signal shows 3.5 clock cycles
- **Clock duty cycle**: time clock is high
  - 50% in this case
- **Clock frequency**: 1/period
  - Above: freq = 1 / 20ns = 50MHz;
The clock shown in the waveform below has:

A. Clock period of 4ns with 250MHz frequency
B. Clock duty cycle 75%
C. Clock period of 1ns with 1GHz frequency
D. A. & B.
E. None of the above
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Latches and Flip-Flops

Tajana Simunic Rosing
Where we are....

• Last time:
  – Memory, SR latch

• Plan for today:
  – Latches and flip flops

• Deadlines coming up:
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Avoiding $S=R=1$ Part 2: Level-Sensitive D Latch

- SR latch requires careful design so $SR=11$ never occurs
- D latch helps by inserting the inverter between $S$ & $R$ inputs
  - Inserted inverter ensures $R$ is always the opposite of $S$ when $C=1$
## D Latch Truth Table

<table>
<thead>
<tr>
<th>CLK</th>
<th>D</th>
<th>( \overline{D} )</th>
<th>S</th>
<th>R</th>
<th>( Q )</th>
<th>( \overline{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>( X )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello & Vahid
D Latch Summary

• Two inputs: \( CLK, D \)
  – \( CLK \): controls \textit{when} the output changes
  – \( D \) (the data input): controls \textit{what} the output changes to

• Function
  – When \( CLK = 1 \),
    \( D \) passes through to \( Q \) (\textit{transparent})
  – When \( CLK = 0 \),
    \( Q \) holds its previous value (\textit{opaque})

• (Mostly) avoids invalid case \( Q = Q' \)
Level-Sensitive D Latches

Assume that data in all latches is initially 0. Input Y=1 and Clk transitions from 0->1. When Clk=0 again, the stored values in latches are:

A. Q1=1, Q2=0, Q3=0, Q4=0 for both clock A & B
B. Q1=1, Q2=1, Q3=1, Q4=1 for clock A
   Q1=1, Q2=0, Q3=0, Q4=0 for clock B
C. Q1=1, Q2=1, Q3=1, Q4=1 for both clocks
D. More information is needed to determine the answer
E. None of the above
**Flip-flop**: Bit storage that stores on the clock edge, not level

- **Master-slave design**: master loads when Clk=0, then slave when Clk=1

Sources: TSR, Katz, Boriello & Vahid
D Flip-Flop: Characteristic Equation

Characteristic Equation

\[ Q(t+1) = D(t) \]
Bit Storage Overview

SR latch

S and R only have effect when C=1. We can design outside circuit so SR=11 never happens when C=1. Problem: avoiding SR=11 can be a burden.

Level-sensitive SR latch

S=1 sets Q to 1, R=1 resets Q to 0. Problem: SR=11 yield undefined Q.

SR can’t be 11 if D is stable before and while C=1, and will be 11 for only a brief glitch even if D changes while C=1. Problem: C=1 too long propagates new values through too many latches: too short may not enable a store.

Only loads D value present at rising clock edge, so values can’t propagate to other flip-flops during same clock cycle. Tradeoff: uses more gates internally than D latch, and requires more external gates than SR – but gate count is less of an issue today.

Sources: TSR, Katz, Boriello & Vahid
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Latches, Flip-Flops
Registers & Counters

Tajana Simunic Rosing
Bit Storage Overview

**SR latch**
- S (set)
- R (reset)
- S=1 sets Q to 1, R=1 resets Q to 0.
- Problem: SR=11 yield undefined Q.

**Level-sensitive SR latch**
- S and R only have effect when C=1. We can design outside circuit so SR=11 never happens when C=1.
- Problem: avoiding SR=11 can be a burden.

**D latch**
- SR can’t be 11 if D is stable before and while C=1, and will be 11 for only a brief glitch even if D changes while C=1.
- Problem: C=1 too long propagates new values through too many latches: too short may not enable a store.

**D flip-flop**
- Only loads D value present at rising clock edge, so values can’t propagate to other flip-flops during same clock cycle.
- Tradeoff: uses more gates internally than D latch, and requires more external gates than SR – but gate count is less of an issue today.

**SRAM cell**
- 6 transistors
- x4 transistors
- B) 2 inputs + 2 transistors
- C) A & B

Sources: TSR, Katz, Boriello & Vahid
Rising vs. Falling Edge D Flip-Flop

Symbol for rising-edge triggered D flip-flop

Symbol for falling-edge triggered D flip-flop

The triangle means clock input, edge triggered

Internal design: Just invert servant clock rather than master

Sources: TSR, Katz, Boriello & Vahid
Enabled D-FFs

• **Inputs:** $CLK, D, EN$
  - The enable input ($EN$) controls when new data ($D$) is stored

• **Function**
  - $EN = 1$: $D$ passes through to $Q$ on the clock edge
  - $EN = 0$: the flip-flop retains its previous state
Additional D-FF Features

- **Reset** (set state to 0) – R
  - synchronous: $D_{new} = R' \cdot D_{old}$ (when next clock edge arrives)
  - asynchronous: doesn't wait for clock

- **Preset or set** (set state to 1) – S (or sometimes P)
  - synchronous: $D_{new} = D_{old} + S$ (when next clock edge arrives)
  - asynchronous: doesn't wait for clock

- **Both reset and preset**
  - $D_{new} = R' \cdot D_{old} + S$ (set-dominant)
  - $D_{new} = R' \cdot D_{old} + R'S$ (reset-dominant)

- **Selective input capability** (input enable or load) – LD or EN
  - multiplexor at input: $D_{new} = LD' \cdot Q + LD \cdot D_{old}$
  - load may or may not override reset/set (usually R/S have priority)

- **Complementary outputs** – Q and Q'
Comparison of latches and flip-flops

- **D** \( \land \) \( \triangleleft \) \( \text{CLK} \)
  - Positive edge-triggered flip-flop

- **D** \( \land \) \( \text{G} \) \( \text{CLK} \)
  - Level-sensitive latch

Sources: TSR, Katz, Boriello & Vahid
D Flip-Flops

Assume that the data in all D-FFs is initially 0. Input Y=1. When Clk goes from 0->1, the stored values in D-FFs are:

A. Q1=1, Q2=0, Q3=0, Q4=0 for both clock A & B
B. Q1=1, Q2=1, Q3=1, Q4=1 for clock A
   Q1=1, Q2=0, Q3=0, Q4=0 for clock B
C. Q1=1, Q2=1, Q3=1, Q4=1 for both clocks
D. More information is needed to determine the answer
E. None of the above
Registers and Counters
Building blocks with FFs: Basic Register
Shift register

- Holds & shifts samples of input
Pattern Recognizer

- Combinational function of input samples
Design of a Universal Shift Register

Sources: TSR, Katz, Boriello & Vahid
Counters

• Sequences through a fixed set of patterns

LFSR

Sequences through a fixed set of patterns.
General Counters

- Default operation: count up
- QA-QD counter output
- A-D parallel load data
- LOAD enables data load
- RCO ripple carry out
- CLR clears data
- EN counter enable

Sources: TSR, Katz, Boriello & Vahid
Finite State Machines
Circuit Specifications

- **Combinational Logic**
  - Truth tables, Boolean equations, logic diagrams (no feedback)

- **Sequential Networks**: State Diagram (Memory)
  - State and Excitation Tables
  - Characteristic Expression
  - Logic Diagram (FFs and feedback loops)

RTL: Register-Transfer Level Description

Sources: TSR, Katz, Boriello & Vahid
Finite State Machines: Two Bit Counter Example

Symbol/ Circuit

2 bit Counter

State Diagram

State Table

<table>
<thead>
<tr>
<th>Current state</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>S₀</td>
<td>S₁</td>
</tr>
<tr>
<td>S₁</td>
<td>S₂</td>
</tr>
<tr>
<td>S₂</td>
<td>S₃</td>
</tr>
<tr>
<td>S₃</td>
<td>S₀</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Q₁(t)</th>
<th>Q₀(t)</th>
<th>Q₁(t+1)</th>
<th>Q₀(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
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</tr>
<tr>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Which is the most likely circuit realization of the two-bit counter?

State Table

<table>
<thead>
<tr>
<th>Q₁(t)</th>
<th>Q₀(t)</th>
<th>Q₁(t+1)</th>
<th>Q₀(t+1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
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<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

A. Combinational circuit

Circuit with no flip flops

B. Circuit with 2 flip flops

C. Circuit with one flip flop

Sources: [TSR, Katz, Boriello & Vahid]
Finite State Machines
Where we are…

• Last time:
  – Memory, latches, flip flops, registers, counters

• Plan for today:
  – FSM

• Deadlines coming up:
  – HW assigned, due Monday at the beginning of the class
    • 4 problems, 2 graded
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• Reminders
  – Discussion session on Friday
Combinational vs. Sequential

• Combinational Logic
  – Truth tables, Boolean equations, logic diagrams (no feedback)

• Sequential Networks: FSMs
  – State and Excitation Tables
  – Characteristic Expression
  – Logic Diagram (FFs and feedback loops)

RTL: Register-Transfer Level Description
Finite State Machine (FSM) Definition

- FSM consists of
  - Set of states
  - Set of inputs, set of outputs
  - Initial state
  - Set of transitions
    - Only one can be true at a time

- FSM representations:
  - State diagram
  - State table

Sources: TSR, Katz, Boriello & Vahid
Watch for transition properties!
(note that more transitions need to be added)
We store the current state using D-flip flops so that:

- Inputs to the combinational circuit don’t change while the next output is computed.
- The transition to the next state only occurs at the rising edge of the clock.

\[
D_0(t) = Q_0(t)'
\]
\[
D_1(t) = Q_0(t) Q_1(t)' + Q_0(t)' Q_1(t)
\]
FSM Controller Design Process with a Three Bit Counter Example

1. State Diagram
2. State Table
3. State Assignments
4. Excitation Table
   (present state, inputs; next state, outputs)
5. Circuit

Excitation Table with Assigned State Patterns

<table>
<thead>
<tr>
<th>C3</th>
<th>C2</th>
<th>C1</th>
<th>N3</th>
<th>N2</th>
<th>N1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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</tr>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Mealy and Moore Machines

Mealy Machine: \( y_i(t) = f_i(X(t), S(t)) \)
Moore Machine: \( y_i(t) = f_i(S(t)) \)

\[ s_i(t+1) = g_i(X(t), S(t)) \]
This Counter Design Is:

A. Moore machine
B. Mealy machine
C. None of the above

Sources: TSR, Katz, Boriello & Vahid
Life on Mars?

Mars rover has a binary input $x$. When it receives the input sequence $x(t-2, t) = 001$ from its life detection sensors, it means that it has detected life on Mars 😊 and the output $y(t) = 1$, otherwise $y(t) = 0$ (no life on Mars ☹).

This pattern recognizer should have
A. One state because it has one output
B. One state because it has one input
C. Two states because the input can be 0 or 1
D. More than two states because ….
E. None of the above
Mars Life Recognizer FSM

Which of the following diagrams is a correct Mealy solution for the 001 pattern recognizer on the Mars rover?

A. [Diagram A]

B. [Diagram B]

C. Both A and B are correct

D. None of the above
What does state table need to show to design controls of C1?
A. (current input $x(t)$, current state $S(t)$ vs. next state, $S(t+1)$)
B. (current input, current state vs. current output $y(t)$)
C. (current input, current state vs. current output, next state)
D. None of the above

Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table with State Assignment

State Assignment
S0: 00
S1: 01
S2: 10

<table>
<thead>
<tr>
<th>S(t)</th>
<th>x</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>S1</td>
<td>0/0</td>
<td>S0,0</td>
</tr>
<tr>
<td>S1</td>
<td>S2</td>
<td>0/0</td>
<td>S0,0</td>
</tr>
<tr>
<td>S2</td>
<td></td>
<td>0/0</td>
<td>S0,1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S(t)</th>
<th>x</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>01</td>
<td>00</td>
<td>00,0</td>
</tr>
<tr>
<td>01</td>
<td>10</td>
<td>00</td>
<td>00,0</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>00</td>
<td>00,1</td>
</tr>
</tbody>
</table>

Q_{1(t+1)}Q_{0(t+1)}, y

Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table => Excitation Table => Circuit

<table>
<thead>
<tr>
<th>Q_1(t)</th>
<th>Q_0(t)</th>
<th>x</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>01,0</td>
<td>00,0</td>
</tr>
<tr>
<td>01</td>
<td>10,0</td>
<td>00,0</td>
</tr>
<tr>
<td>10</td>
<td>10,0</td>
<td>00,1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>id</th>
<th>Q_1Q_0x</th>
<th>D_1</th>
<th>D_0</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>000</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>001</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>010</td>
<td>1</td>
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<td>0</td>
</tr>
<tr>
<td>3</td>
<td>011</td>
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<td>0</td>
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<td>100</td>
<td>1</td>
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<td>0</td>
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<td>1</td>
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<td>6</td>
<td>110</td>
<td>X</td>
<td>X</td>
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<tr>
<td>7</td>
<td>111</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello & Vahid
Finite State Machines

CSE 140
Prof. Tajana S. Rosing
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• Last time:
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  – FSMs & timing
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  – Discussion session on Friday
  – Exam #2 Feb 27th
State Diagram $\Rightarrow$ State Table $\Rightarrow$ Excitation Table $\Rightarrow$ Circuit

<table>
<thead>
<tr>
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Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table => Excitation Table => Circuit

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D_1(t):  

\[
D_1(t) = x'Q_0 + x'Q_1
\]

D_0(t) = Q_1Q_0' x'

y = Q_1x'

Sources: TSR, Katz, Boriello & Vahid
State Diagram => State Table => Excitation Table => Circuit

\[ D_1(t) = x'Q_0 + x'Q_1 \]
\[ D_0(t) = Q'_1Q'_0 x' \]

\[ y = Q_1x \]
Moore FSM for the Mars Life Recognizer

Which of the following diagrams is a correct Moore solution to the ‘001’ pattern recognizer?

A. 1/0

B. 1

C. Both A and B are correct

D. None of the above
Moore Mars Life Recognizer: FF Input Specs

Pattern Recognizer ‘001’

Moore Machine

What does state table need to show to design controls of C2?
A. (current input $x(t)$, current state $S(t)$ vs. next state, $S(t+1)$)
B. (current input, current state vs. current output $y(t)$)
C. (current state vs. current output $y(t)$ and next state)
D. (current state vs. current output $y(t)$)
E. None of the above
Moore Mars Life Recognizer: State Table

<table>
<thead>
<tr>
<th>ID</th>
<th>$Q_1Q_0x$</th>
<th>$D_1$</th>
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S(t)$x$

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$Q_1(t+1)Q_0(t+1)$, $y$
### Mars Life Recognizer: Combinational Circuit Design

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**D1(t):**

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**D0(t):**

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**y(t):**

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**x(t):**

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Sources: TSR, Katz, Boriello, Vahid
Mars Life Recognizer Circuit Implementation

State Diagram => State Table => Excitation Table => Circuit

State Diagram:
- Input: A
- Clock: B
- Output: C
- Initial State: D
- Next State: E

Transitions:
- A → D
- B → C

Moore Machine:
- Inputs: x(t)
- Outputs: y(t)
- Clock: CLK
- States: S(t)

Circuit Diagram:
- D0 to D1
- Q0 to Q1
- y

Sources: TSR, Katz, Boriello & Vahid
15 cents for candy! Watch out – no change!

- **Moore machine**
  - outputs associated with state

- **Mealy machine**
  - outputs associated with transitions

Sources: TSR, Katz, Boriello & Vahid
Example: Moore implementation

- Encode states and map to logic

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<th>output</th>
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open = Q1 Q0
Example: Mealy implementation

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Sources: TSR, Katz, Boriello & Vahid
Timing Constraints in Sequential Designs
Our seemingly logically correct design can go wrong – signals don’t travel in zero time 😞

- We next look at timing constraints for combinational and sequential logic.
I. Min delay of a gate, also called contamination delay: $t_{cd}$
   Minimum time from when an input changes until the output starts to change

II. Max delay of a gate, also called propagation delay: $t_{pd}$
   Maximum time from when an input changes until the output is guaranteed to reach its final value (i.e., stop changing)
Which path in the above circuit determines the contamination delay of the circuit (assuming the delay of all the gates is the same)?

A. Blue path
B. Red path
C. Both
D. Neither
Which path in the above circuit determines the propagation delay of the circuit (assuming the delay of all the gates is the same)?

A. Blue path  
B. Red path  
C. Both  
D. Neither
D-FF Input Constraints: Setup and Hold Times

I. Setup time: $t_{\text{setup}}$
   Time \textit{before} the clock edge that data must be stable (i.e. not change)

II. Hold time: $t_{\text{hold}}$
   Time \textit{after} the clock edge that data must be stable

Aperture time: $t_a$
Time around clock edge that data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)
Output Timing Constraints

I. Min delay of FF, also called contamination delay or min CLK to Q delay: $t_{ccq}$
   Time after clock edge that $Q$ might be unstable (i.e., starts changing)

II. Max delay of FF, also called propagation delay or maximum CLK to Q delay: $t_{pcq}$
    Time after clock edge that the output $Q$ is guaranteed to be stable (i.e. stops changing)
The timing of which of the following signals can cause a setup-time violation?

A. The input signal D(t)
B. The output signal Q(t)
C. Both of the above
D. None of the above
Causes of Timing Issues in Sequential Circuits

- Input to a FF comes from the output of another FF through a combinational circuit
- The FF and combinational circuit have a min & max delay

\[
\text{CLK} \quad \begin{array}{c}
\text{Q1} \\
\hline
\text{R1} \\
\hline
\end{array} \quad \text{C} \quad \begin{array}{c}
\text{D2} \\
\hline
\text{R2} \\
\hline
\end{array} \quad \text{CLK}
\]

Which of the following violations occurs if max delay of R1 is zero & max delay of the combinational circuit is equal to the clock period?

A. Hold time violation for R2
B. Setup violation for R2
C. Hold time violation for R1
D. Setup violation for R1
E. None of the above

Sources: TSR, Katz, Boriello & Vahid
Setup Time Constraint

- Input to a FF comes from the output of another FF through a combinational circuit.
- The FF and combinational circuit have a min & max delay.

Setup time constraint:

\[ T_c \geq t_{\text{setup}} + \text{max delay(FF)} + \text{max delay(combinational)} \]

\[ T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} \]
Causes of Timing Issues in Sequential Circuits

- Input to a FF comes from the output of another FF through a combinational circuit
- The FF and combinational circuit have a min & max delay

Which of the violations would occur if the min delay of R1 was zero and the combinational circuit was just a wire?

A. Hold time violation for R2
B. Setup violation for R2
C. Hold time violation for R1
D. Setup violation for R1
E. None of the above
Hold Time Constraint

• Input to a FF comes from the output of another FF through a combinational circuit
• The FF and combinational circuit have a min & max delay

\[
\text{Hold time constraint:} \\
\quad t_{\text{hold}} < \min \text{ delay(FF)} + \min \text{ delay(combinational)} \\
\quad t_{\text{hold}} < t_{ccq} + t_{cd}
\]
Once a flip flop has been built, its timing characteristics stay fixed: $t_{\text{setup}}$, $t_{\text{hold}}$, $t_{\text{ccq}}$, $t_{\text{pcq}}$

What about the clock? Does the clock edge arrive at the same time to all the D-FFs on the chip?
Clock Skew

- The clock doesn’t arrive at all registers at the same time
- **Skew**: difference between the two clock edges
- Perform the **worst case analysis**

![Diagram of clock skew](image)

Sources: TSR, Katz, Boriello & Vahid
Setup Time Constraint with Skew

- In the worst case, CLK2 is earlier than CLK1
- $t_{pcq}$ is max delay through FF, $t_{pd}$ is max delay through logic

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew})$$
Hold Time Constraint with Skew

- In the worst case, CLK2 is later than CLK1
- $t_{ccq}$ is min delay through FF, $t_{cd}$ is min delay through logic

\[
 t_{ccq} + t_{cd} > t_{hold} + t_{skew} \\
 t_{cd} > t_{hold} + t_{skew} - t_{ccq}
\]
Timing Analysis Example

Timing Characteristics

- $t_{ccq} = 30$ ps
- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps per gate
- $t_{cd} = 25$ ps per gate

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = \frac{1}{T_c} = 4.65 \text{ GHz}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} ?$$

$$(30 + 25) \text{ ps} > 70 \text{ ps} ? \text{ No!}$$

Sources: TSR, Katz, Boriello & Vahid
Timing Analysis Example

Add buffers to the short paths:

Add buffers to the short paths:

Timing Characteristics

- $t_{ccq} = 30$ ps
- $t_{pcq} = 50$ ps
- $t_{setup} = 60$ ps
- $t_{hold} = 70$ ps
- $t_{pd} = 35$ ps
- $t_{cd} = 25$ ps

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} \ ?$$

$$(30 + 50) \text{ ps} > 70 \text{ ps} \ ? \ Yes!$$

Sources: TSR, Katz, Boriello & Vahid
Sequential Circuit Design Summary

• SRAM memory, SR Latch, D Latch, D-FF
• Design procedure for FSMs
  1. Capture FSM
  2. Create state table
  3. Assign the states
  4. Excitation table
  5. Implement the combinational logic
• Mealy vs. Moore FSM
• Non-ideal properties of FFs
  – Setup/hold time constraints
  – Maximum operating frequency
  – Clock skew
MORE EXAMPLES
New FF Design

Sources: TSR, Katz, Boriello & Vahid
Counter Design

\[\text{XOR}\]

\[\text{clock} \quad \text{dff0} \quad \text{dff1} \quad \text{dff2}\]
Design FSM with Minimum Number of States

- If two inputs are equal during any four consecutive clock cycles, $w_1 = w_2$, the circuit produces output $z=1$; else, $z=0$. 
FSM Design

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<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Input: a
Output: y

Sources: TSR, Katz, Boriello & Vahid
# FSM Analysis

<table>
<thead>
<tr>
<th>Q1Q0A</th>
<th>Q1(t+1)</th>
<th>Q0(t+1)</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>010</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>011</td>
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<tr>
<td>111</td>
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</table>
FSM design: Multiple input counter

- Given FSM of a multiple input counter, design the circuit implementing its functionality.

\[
\begin{array}{c|c|c|c|c|c}
\text{present state} & S0 & S1 & S2 & S3 \\
\hline
00 & S0 & S1 & S2 & S3 \\
01 & S0 & S3 & S1 & S3 \\
11 & S1 & S0 & S0 & S3 \\
10 & S1 & S3 & S2 & S0 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c|c|c}
\text{output} & 00 & 01 & 10 & 11 & \\
\hline
1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 \\
\end{array}
\]
Multiple input counter: Logic for D-FF

- Derive logic equations for inputs of D-FF

<table>
<thead>
<tr>
<th>Input</th>
<th>State</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>01</td>
<td>01</td>
<td></td>
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<tr>
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<tr>
<td>10</td>
<td>10</td>
<td>01</td>
<td>00</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

**D1**

<table>
<thead>
<tr>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**D0**

<table>
<thead>
<tr>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Sources: TSR, Katz, Boriello & Vahid
ALU: Minimum POS of Decoder-Mux Circuit