1. Use minimum number of D flip-flops and logic gates to design a counter that produces the following repeating sequence: “0 → 1 → 2 → 4 → 6 → 0 → ...”. For this end,
(a) Show the state-table of the counter.
(b) Show and simplify the K-Map for each flip-flop.
(c) Examine the self-correctness of your machine. In other words, check whether the unused states (3, 5, and 7) have transition to a valid/known state.
(d) Implement the circuit derived in (b).
2. Design a Moore FSM and implement the corresponding sequential circuit that gets an input serially (starting from least significant bit) and serially outputs the two’s complement. Use minimum number of gates and flip-flops. Briefly explain the underlying algorithm of your FSM.
3. The following is a schematic of a T flip-flop, which is made up of a D flop-flop and an XOR gate.

(a) Tabulate the characteristics table of the T flip-flop.

(b) The following counter is build up of the aforementioned T flip-flops and a D flip-flop. Assuming the counter starts with 0000, find out the sequence generated by the counter. Q3 is the most significant bit and F_in is the clock. The reset input (CLR) of the T flip-flops is asynchronous.

(c) Assuming the input clock (F_in) frequency is 21,120 Hz, what is the output frequency, f_out?
4. For the following circuit, assume a clock-to-Q delay of 50ps, setup-time of 20ps, and AND and XOR gate delays of 20ps and 30ps, respectively.

(a) Calculate the minimum clock period. Show all your computation.

(b) Assume that the flip-flops are flawed and require a large hold-time of 200ps. With a buffer delay of 20ps, fix the hold-time violation of the above circuit.

(c) Obtain the minimum clock period of the new (fixed) circuit.