## Instructions

1. Write your name on every page.
2. Please make sure your writing is clear and readable.
3. Show your work.
4. This exam allows only one 8.5 x 11 inch cheat sheet with handwritten notes on both sides. **No electronics** are allowed.
5. Please sign the statement below before you begin:

## Honor code

By signing my name below I hereby certify that I have neither given, nor received assistance in completing this examination:

____________________________________________________
Problem 1. Timing models [15]

A. Show the time evolution of the following distributed events using Vector time. [5]
B. Consider the following Esterel Code. Draw the equivalent FSM. [10]

```
loop
  abort
  await S;
  emit A;
end
loop
  await R;
  abort
  present X then emit B end
  pause;
end
when Y;
  emit C;
end
when Z
end
```
Problem 2. Petri Nets [15]

Assume you have a Petri Net $N$, with $P$ places, $T$ transitions, $F$ flows and $W$ weights:

$P = \{P_1, P_2, P_3, P_4\}$

$T = \{T_1, T_2, T_3\}$

$F = \{(P_1, T_1), (P_1, T_2), (P_2, T_3), (T_1, P_2), (T_3, P_3), (P_3, T_2), (T_2, P_4), (P_4, T_3)\}$

Initial marking $M_0 = [2, 1, 2, 0]$

a) Draw the specified Petri Net. [5]

b) Assume all weights are 1. How many other states are reachable from $M_0$? Show your work. [5]
c) Indicate the liveness of each transition [3]:

   i)  \( T_1: \) ___________

   ii) \( T_2: \) ___________

   iii) \( T_3: \) ___________

d) What degree of liveness does the Petri Net have? [2]
Problem 3. Task Scheduling [15]

Consider the following list of operations. Note that the variables starting with “i” are inputs and the ones starting with “o” are the outputs; and all the other ones are just intermediate variables. Also, a multiplier takes 2 cycles whereas an adder takes 1 cycle to produce the output. Multipliers and adders can operate on 2 operands at once.

1. \( x_1 = i_1 + i_2; \)
2. \( x_2 = i_4 * (i_1 + i_3); \)
3. \( x_3 = i_5 * i_6; \)
4. \( x_4 = x_1 + i_7; \)
5. \( x_5 = x_3 - x_4; \)
6. \( o_1 = x_2 + i_8; \)
7. \( o_2 = x_5 * i_3; \)
8. \( o_3 = i_8 * i_9; \)

a) Give the ASAP schedule assuming no resource constraints. [5]
b) Give the **ALAP** schedule assuming no resource constraints. [5]

c) Give the List schedule assuming that you have only 1 adder and 1 multiplier. [5]
Problem 4. EDF/RM Scheduling [20]

You are given 3 periodic tasks to run on a single processor.

Task A has execution time $C_1 = 2$ and period $P_1 = 7$
Task B has execution time $C_2 = 1$ and period $P_2 = 5$
Task C has execution time $C_3 = 2$ and period $P_3 = x$

Hint: $2^{1/2} \approx 1.414; 2^{1/3} \approx 1.260; 2^{1/4} \approx 1.189; 2^{1/5} \approx 1.149$

a) Assume all tasks arrive at $t=0$. Construct a static RM schedule for this system in the order of task priority. What is the minimum period of $C$ such that it is schedulable? [10]

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b) Assume all tasks arrive at $t=0$. Construct a EDF schedule for this system in the order of task priority. What is the minimum period of $C$ such that it is schedulable? [10]

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Problem 5. StateChart to FSM [15]

Given the following StateChart, draw the equivalent FSM.
Problem 6. SDF [20]

Given the SDF above, answer the following questions.

a) Write the incidence matrix. [4]
b) Find value of \( x \) so that the SDF has a PASS schedule. Write your PASS schedule. Assume that the tasks are executed in the following order: A, B, C, D. [8]
\[ x = \] 
PASS schedule = ________________________________

c) For your PASS schedule, what is the number of initial elements required in each buffer? [4]

d) For your PASS schedule, what is the minimum size needed of each buffer? [4]
Problem 7. BONUS QUESTION [15 pts]:

For each statement, please indicate whether it is True (T) or False (F).

1. Digital signal processors (DSPs) often have optimized arithmetic units that can complete multiply and add operations in sequence in the same cycle.
   T / F

2. Scratchpads are used for their uniform access times vs. the variable access times in a cache hierarchy.
   T / F

3. A common problem in non-volatile memory (NVM) technologies is that write operations cost more than reads, in terms of time and power consumption.
   T / F

4. Compared to floating point number representation, fixed-point design is an effective way to speed up computation at a cost in accuracy.
   T / F

5. Quantization errors can be prevented by sampling above the Nyquist Frequency.
   T / F

6. Pulse width modulation (PWM) is a digital technique for simulating analog signals.
   T / F

7. Rate Monotonic (RM) scheduling has higher runtime overhead than Earliest Deadline First (EDF).
   T / F

8. In real time operating systems, all hardware interrupts must be handled immediately to ensure applications meet their deadlines.
   T / F

9. Mutexes ensure that at most one thread can access a shared variable at any time. Hence, they can prevent deadlocks.
   T / F

10. Esterel is a synchronous reactive language where signals are assumed to arrive instantaneously.
    T / F

11. Specification & Description Language (SDL) is an asynchronous language where messages are assumed to arrive at a node after some possible delay.
    T / F

12. Petri Nets provide deterministic models for a given initial marking.
    T / F

13. With vector time, nodes have full knowledge of all task orderings in a distributed system.
    T / F

14. In a time-division multiple access (TDMA) bus protocol, high priority tasks cannot preempt low priority tasks for a time slot.
    T / F

15. In PID control, a high constant of proportionality on the derivative term (K_d) helps a controller recover quickly from systematic bias.
    T / F