1. Given the partition, perform state partitioning on the following FSM. Use the idle state SA for the left part and idle state SB for the right part.

2. Consider following sequential circuit with one input X and one output Y. Derive the state table and state diagram. Assume initial state of 00.
3. All delays are in nanoseconds. Assume $t_{\text{skew}} = 0$ unless otherwise stated. (Note that buffer has the delay of two inverters).

**FFs:**
- $t_{\text{setup}} = 30$
- $t_{\text{hold}} = 30$
- $t_{\text{coq}} = 10$
- $t_{\text{pcq}} = 20$

**Inverters:**
- $t_{\text{cd}} = 10$
- $t_{\text{pd}} = 15$

**Gates:**
- $t_{\text{cd}} = 15$
- $t_{\text{pd}} = 25$

---

<table>
<thead>
<tr>
<th>$Q_1(t)$</th>
<th>$Q_0(t)$</th>
<th>$X$</th>
<th>$Q_1(t + 1)$</th>
<th>$Q_0(t + 1)$</th>
<th>$Y$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

![Circuit Diagram](image-url)
a. Complete the timing diagram below for the path from FF2 to FF4. Do the inputs satisfy the setup condition? If not, complete the diagram as if it did.

b. Are there any hold violations? Explain each one, or if there are none explain why there are no violations.

c. Fix any hold violations you found. Draw the resulting timing diagram.

d. Given your modified circuit, what is the maximum possible clock frequency? Show your work.

e. If $t_{skew} = 10$, how will the maximum frequency change? Will there be more hold violations? Explain.
4. Consider the following Moore FSM with,
States: $S_0 - S_7$.
Input: $X$.
Output: $Y$.

(a) Perform one-hot state assignment and show the encoding for each state.

(b) How many D-FFs will be required if we have to represent the encoding in part (a)
using a circuit?

(c) Apply the Bit Change heuristic to minimize the number of state bit changes and show
the new state assignments. (Start with $S_0$ as all 0s). Count the total number of bit
changes across all transitions.

(d) How many D-FFs will be required if we have to represent the encoding in part (c)
using a circuit?