1. Consider the following FSM:

A. Which pattern does this FSM recognize?
B. Write an excitation table by using the following state encoding: S0 = 00, S1 = 01, S2 = 10, S3 = 11
C. Use k-maps to implement the state and output logic. Write the minimum expressions for the next state and output.
D. Draw the circuit diagram assuming you have two D-FF and minimum number of gates.
2. Given the following circuit, with one input x and two SR-Latches for Q0 and Q1 and an output y.

a. Fill the excitation table below.

<table>
<thead>
<tr>
<th>id</th>
<th>Q₁(t)</th>
<th>Q₀(t)</th>
<th>x</th>
<th>Q₁(t+1)</th>
<th>Q₀(t+1)</th>
<th>y</th>
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<tbody>
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b. Derive the equations for the following
   (i) Q₁(t + 1) = ______________
   (ii) Q₀(t + 1) = ______________
   (iii) y(t) = ______________

c. Come up with the state diagram.
3. Consider a sequential circuit that outputs $Y = 1$ when it receives input sequence $X(t-3, t) = 0010$ (recognizes input sequence 0010).
   a. Draw a Mealy FSM with minimum number of states.
   b. Draw a Moore FSM with minimum number of states.
   c. Which version of FSM requires more transistors?

4. Consider the following circuit.

Suppose
   - each AND and OR gate has a $t_{pd} = 30$ps, $t_{cd} = 20$ ps
   - the NOT gate has $t_{pd} = 20$ps, $t_{cd} = 15$ps
   - each flip-flop has a $t_{pcq} = 35$ps, $t_{ccq} = 30$ps, $t_{setup} = 30$ps, $t_{hold} = 40$ps

   a. Which paths determine the contamination delay? Draw it on the circuit with a blue line.
   b. Which paths determine the propagation delay? Draw it on the circuit with a red line.
   c. Suppose there is no clock skew. What is the maximum operating frequency?