CSE140: Components and Design Techniques for Digital Systems

Midterm #2 Sample Problems

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Where we are now…

• What we have covered:
  – Combinational and sequential circuits up to & including FSMs

• What we’ll do today:
  – Midterm review

• Deadlines:
  – HW#4 due today, solutions posted Friday at 2pm
  – Midterm #2 on Saturday at 1pm
    • All material up to and including today
    • Bring one 8 ½ x 11” paper with handwritten notes, but nothing else

• TA/Tutor extra office hours through Saturday morning
  – See piazza post for more details

• Prof. office hours Thursday 5pm – as long as it takes 😊
What does this circuit do?

Is this circuit:
A. Latch
B. Flip-flop
C. None of the above
FSM design example

• Design an overlapping finite string pattern recognizer
  – output is 1 whenever the input sequences 101 and 011 are observed
# FSM Analysis

<table>
<thead>
<tr>
<th>A</th>
<th>Q1Q0</th>
<th>Q1(t+1)</th>
<th>Q0(t+1)</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001</td>
<td></td>
<td></td>
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<tr>
<td>010</td>
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<td></td>
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<tr>
<td>011</td>
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<tr>
<td>100</td>
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</tr>
<tr>
<td>101</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>110</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>111</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

A Q1Q0: A Q1Q0 (Input States)  
Q1(t+1): Q1 Next State  
Q0(t+1): Q0 Next State  
Y: Output
Minimum POS of Decoder-Mux Circuit

This design has:
A. 2 inputs & 1 output
B. 4 inputs & 1 output
C. 2 states; output is Moore
D. B. & C.
E. None of the above
Sequential circuit design

The following is true for this design:
A. It has one output that is Mealy
B. It has two states, each can be 0 or 1
C. It has no inputs
D. None of the above

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next state W=0</th>
<th>Next state W=1</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>10</td>
<td>11</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>00</td>
<td>00</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>00</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>00</td>
<td>1</td>
</tr>
</tbody>
</table>
What does this circuit do?

The following is true for the circuit on the left:
A. Moore outputs
B. It has one input
C. All of the above
D. None of the above
What does this circuit do?

Assume that both D-FFs are reset at start

The following is true for the circuit on the left:
A. It has Moore outputs
B. It has a mux
C. It has one input
D. It uses a decoder
E. None of the above
Logic & Timing diagrams
ALU design

• Design at 2 bit ALU using the specification given below with maximum two full adders and minimum number of other elements

<table>
<thead>
<tr>
<th>$S_1$</th>
<th>$S_0$</th>
<th>ALU Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$F_i = (A_i == B_i)$ (bitwise equality)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$F_i = (A_i &lt; B_i)$ (bitwise strictly less than)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$F_i = A_i + B_i + 1$ (addition, then increment)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$F_i = A_i - B_i - 1$ (subtraction, then decrement)</td>
</tr>
</tbody>
</table>