Week 8 Discussion

Shubham Gupta
Topics:

- RTL
  - HLSM
  - Data Path
  - HLSM -> FSM
  - Controller

- Problems!
RTL Design Process

- Create a HLSM diagram to describe the problem
- Then we convert it to a circuit. How?
  - Create a datapath
  - Connect datapath and controller
  - Derive the controller’s FSM
  - Create a circuit for FSM
Let’s design a Treadmill!

Design a system to control the speed of the conveyer belt on the treadmill.

Speed is a 8 bit value which can be controlled with two button: UP and DOWN.

UP increases the speed by 1, DOWN decreases the speed by 1. If both of them are pressed, no change in speed occurs. So,

INPUTS: bit UP, bit DOWN

OUTPUT: byte SPEED

NOTE: Don’t forget to initialize the speed. :)
HLSM Diagram!

Speed: Saves the speed

Init: Initializes speed to 0

Wait: Waits for UP or DOWN signal

INCR/DECR:
Increment/decrement value of Speed
Datapath:
Datapath:

SPEED_REG: Register to store speed

Register takes ld and clr signals.

Incrementor/Decrementor is made up of Adders and MUX!

Changes value of Speed depending on up_down signal

Output is obtained from SPEED_REG!!
Connecting Controller to Datapath:
Replace data operations with setting and reading of control signals to and from the datapath.
From here, can you convert it to a circuit?
Timing!

We need to make sure there are no Hold/setup time violations!

Do you see any potential path where there could be a violation?
Consider this circuit.

Rectangle: Combinational logic.

What is the longest path?
Consider this circuit.

Rectangle: Combinational logic.

What is the longest path?

We need to look at each **fully combinational path** from output of one FF to input of another FF.

Fully combinational means there should not be any FF in the middle!
From FF1 to FF2: Path A
From FF2 to FF1: Path C
From FF1 to FF3: Path A + B

Any more?
Timing!

From FF1 to FF2: Path A
From FF2 to FF1: Path C
From FF1 to FF3: Path A + B

Any more?

Yes!

From FF4 to FF4! Path D.

Also, if two FF are connected to each other, that path will be shortest.
Find the shortest and the longest path in the circuit.

Make sure there are no violations! :)

\[ T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew} \]

\[ t_{ccq} + t_{cd} > t_{hold} + t_{skew} \]
Incrementor/Decrementor is made up of MUX and ripple carry adder.

Here, we assume that for MUX, \( T_{pd} = 10 \) \( \text{us} \)

Assume delay of RC adder = 32 \( \text{us} \).
(How? We'll see in a second!)
Incrementor/Decrementor is made up of MUX and ripple carry adder.

Here, we assume that for MUX, $T_{pd} = 10$ us.

Assume delay of RC adder = 32 us. (How? We'll see in a second!)

What is the Critical path in the ckt shown?
Here, we assume that for MUX, $T_{pd} = 10$ us

Ripple carry adder is made up of 8 full adders. Assume each gate in adder has a $T_{pd} = 2$ us.

For $n$ Full adders, number of gates in critical path = $2 \times n$
Here, we assume that for MUX, $T_{pd} = 10$ us.

Ripple carry adder is made up of 8 full adders. Assume each gate in adder has a $T_{pd} = 2$ us.

For $n$ Full adders, number of gates in critical path = $2 \times n$

For 8 Full Adders in RC adder, number of gates in critical path = $2 \times 8 = 16$

So, delay of RC Adder = $16 \times 2 \text{ us} = 32$ us.
Find all the paths between FFs!
Find all the paths between FFs!
Find all the paths between FFs!
Find all the paths between FFs!
Find all the paths between FFs!
Find all the paths between FFs!