
   A. Implement the following function using the template of 2:1 Multiplexers given.
   NOTE: They are either one of the literals, 1 or 0.

   ![Multiplexer Diagram]

   B. Implement the function using minimum number of 2:4 decoders and other gates.

2. Consider the following incomplete state diagram and excitation table with one 1-bit input and one 1-bit output. The FSM detects the pattern “1101” (repeating pattern allowed) and outputs a 1 when the pattern is detected.

   Example:

   | x  | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
   |----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
   | Z  | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
a. Is this Mealy or Moore machine?
b. Complete the above state diagram.
c. Using binary state assignments (e.g. $S0=00$, $S1=01$,...), complete the excitation table with current state, inputs, next state and output.

d. Use k-map to derive the equation for $D1(MSB)$ and output $Z$.
e. Implement the logic for $D1(MSB)$ and output using D-FF and minimum number of other multiple-input gates.

3. Consider the following code.
Inputs: byte Mem[10], byte A, bit in, bit r
Output: bit equal
i = 0;
equal = 0;
while(1) {
    if in == 1 {
        while (in == 1) {}
        if Mem[i] != A {
            i = 0;
        } else {
            i = i + 1
        }
    }
    if r == 1 {
        while (r == 1) {}
        i = 0;
    }
    if i == 10 {
        equal = 1;
        break;
    }
}

a. Briefly describe what this code does.
b. Draw a HLSM that captures the functionality of the code.
c. Create a datapath for this system.
d. Show connections between datapath and controller. Label all the signals.

4.
A. Consider the circuit below.
The elements of the circuit have the following timing characteristics:
For Flip Flop: $T_{pcq} = 50\text{ps}, T_{ccq} = 20\text{ps}, T_{\text{setup}} = 25\text{ps}, T_{\text{hold}} = 30\text{ps}$
All logic gates, $T_{pd} = 25\text{ps}, T_{cd} = 15\text{ps}$
And has zero clock skew.

(i) What is the maximum clock frequency for the circuit?
(ii) How much clock skew can the circuit tolerate before it experiences a hold time violation?

B. Consider the following circuit with a NOR-based SR-latch and a D-FF. Timing information is as follows:

Propagation delay for the FF: 0.5 ns
Propagation delay for all gates (except ones in the FF): 0.5 ns
Clock period = 4 ns
Complete the waveforms below.

```
<table>
<thead>
<tr>
<th>t = 0</th>
<th>0.5 ns</th>
<th>4 ns</th>
<th>t = 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q'</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```