1. Design a system that repeatedly computes and outputs the maximum value found within a register file A consisting of 64 32-bit integers.

2. Use the RTL design process to create an alarm system that sets a single bit output ALARM to 1 when the average temperature of four consecutive samples meets or exceeds a user defined threshold value. A 32-bit unsigned input CT indicates the current temperature, and a 32-bit unsigned input WT indicates the warning threshold. Sample should be taken every few clock cycles. A single bit input clr when 1 disables the alarm and sample process. Start by capturing the desired system behavior as an HLSM, and then convert to a controller/datapath.

3. Convert the following C code to HLSM.

   Inputs: byte a[256], byte b, bit go
   Outputs: byte freq, bit done
   FREQUENCY:
   while(1){
     while(!go);
     done = 0;
     i = 0;
     freq = 0;
     while(i < 256){
       if (a[i] == b){
         freq = freq + 1;
       }
       i = i + 1
     }
     done = 1;
   }

4. Use RTL design process to create the following system. The system receives a 4 bit number A as an input whenever signal u = ‘1’. The 8-bit output S is the sum of all the input numbers up to now. Input r =’1’ is used to reset S to 0. You may assume that overflow does not occur.

   a. Draw HLSM for the system. Hint: you only need 3 states to capture the system behavior.
   b. Design the system datapath. Clearly show the signals that need to be generated by controller.
c. Draw the **Moore** FSM corresponding to the controller.

d. Complete the excitation table for the system. Use minimum bit-change state assignment strategy to encode states. Use code 00 for the init state, and code 01 for wait (idle) state.

e. Implement the controller FSM using flipflops and minimum number of 2-input gates to generate the required control signals.

f. Assuming all gates (regardless of number of inputs) have 2ns delay and we have used ripple-carry adder in datapath, find the critical path for the system. (Wires have no delay)

g. Calculate the maximum clock frequency for the circuit.

Flipflop timing characteristics:

\[ t_{\text{setup}} = t_{\text{hold}} = 6\text{ns} \]
\[ t_{\text{ccq}} = 8\text{ns} \quad t_{\text{pcq}} = 12\text{ns} \]