1. Design a sequential pattern recognizer with a single input $x$ and has a single output $y$ that outputs a logic 1 when a pattern “0101” is observed, and otherwise outputs a zero. (50 pts)
   A. Using shift register
   B. In this part, you will design an FSM with D-FFs which recognizes the pattern.
      I. Draw FSM assuming mealy implementation with minimum number of states.
      II. Use binary encoding for states. Eg. if the circuit needs 4 D-FFs, the state $S_0$ would be 0000, $S_1$ will be 0001 and so on. Using this state encoding, write down the excitation table which has input, current state, output and next state.
      III. Using K-Maps, minimize logic for output and next state.
      IV. Draw the circuit implementation using D-FFs and minimum number of other gates.

2. The sequential circuit below has one D flip flop, one full adder and two inputs $x$ and $y$. The circuit adds $x$, $y$, and the carry-out of the previous sum. Given the circuit, derive state table and state diagram. (50 pts)
3. Design an ALU with two 4-bit inputs A and B, and control inputs M2,M1,M0. The ALU should support the operations as stated in the table below. Use no more than one Adder, one 4:1 Multiplexer and three 2:1 multiplexers. (50 pts)

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Operation</th>
<th>Output F=</th>
</tr>
</thead>
<tbody>
<tr>
<td>M2</td>
<td>M1</td>
<td>M0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>

4. (50 points)

a) Analyze the following SR NAND latch by filling the given truth table. Clearly identify different latch states. (10 points)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
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<td>0</td>
<td>1</td>
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<td>0</td>
<td>0</td>
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</tr>
</tbody>
</table>
b) We use a SR NAND latch (similar to part a) alongside a D Flip-Flop to create the following circuit. Trace the behavior of the circuit and complete the timing diagram. Initially, \( Q_1 = 1 \) and \( Q_2 = 0 \). (40 points)