In this homework, we practice the analysis and synthesis of sequential networks. For the first problem, we draw the timing diagram of the latch and flip-flop. For the second problem, we translate a pattern recognizer into state diagrams and state tables. For the third problem, we analyze the behavior of a sequential circuit. For the last problem, we design the circuit from a given description.

1. Timing Diagram of Latch and Flip-Flop: Given the input waveforms shown below, sketch the outputs.

<table>
<thead>
<tr>
<th></th>
<th>CLK</th>
<th>D</th>
<th>D-latch</th>
<th>D-FF</th>
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<td><img src="image" alt="Waveform Diagram" /></td>
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</table>
2. A sequential network has one binary input \( x(t) \) and one binary output \( y(t) \). The network produces \( y = 1 \), whenever input pattern \( x(t - 2, t) = 100 \) or \( 110 \). Otherwise, the output \( y = 0 \).

2.1 Design the system as a Mealy machine with a minimal number of states.
   (i) Draw the state diagram.
   (ii) Write the state table.

2.2 Design the system as a Moore machine with a minimal number of states.
   (i) Draw the state diagram.
   (ii) Write the state table.

3. Given the circuit as described in zyBook 3.8.2, replace the state register with two T flip-flops.
   (i) Write the state table.
   (ii) Draw the state diagram.

4. A state machine has one input \( x(t) \) and two-bit state \((Q_1(t), Q_0(t))\). The machine is described by the following state equations.
   \[
   Q_1(t+1) = Q_0(t) + x'(t)Q_1'(t),
   Q_0(t+1) = Q_1'(t) + x(t)Q_0(t),
   y(t) = Q_1(t)Q_0(t)
   \]
   Use two JK flip-flops and a minimal two-level NAND network to implement the machine.
(i). Write the state excitation table and draw the state diagram.
(ii). Show your derivation (K maps) and draw the logic diagram.