1. Universal Set of Gates:
   1.1. State the definition of universal set of gates (8 points).

1.2. Check if the set in the following list is universal and explain your decision. Assuming constants 0 and 1 are available as inputs (12 points).
   1.2.1. \{OR, NOT\}
   1.2.2. \{NAND, NOR\}
   1.2.3. \{f(x, y)\}, where \(f(x, y) = x'y\)
   1.2.4. \{f(x, y, z)\}, where \(f(x, y, z) = (x'y' + xy)z\)
2. Other Types of Gates: Prove or disprove using Boolean algebra the following statement (15 points).

If $AB = 0$ then $A \oplus B = A + B$. 
3. Timing Diagram of Latch and Flip-Flop:
3.1 Given the input waveforms shown below, sketch the output, $Q$, of a D latch (10 points).

3.2 Given the input waveforms shown below, sketch the output, $Q$, of a D flip-flop (10 points).
4. (Finite State Machine Specification) Analyze the following circuit.

4.1 Write the transition(excitation) table (8 points).
4.2 Sketch the state diagram. Assign the initial state $S_0$ as 00. (7 points).

4.3 Fill the following table and describe in words what the finite state machine does (5 points).

<table>
<thead>
<tr>
<th>cycle</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>$X$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>state</td>
<td>$S_0$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$M$</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
5. (Flip-Flops) Implement a T flip-flop with a D flip-flop and a minimal AND-OR-NOT network. Let us assume that the complements of T, D and Q signals are available. Draw the logic diagram to show your design (25 points).