CSE 141:
Computer Architecture
Professor: Michael Taylor

UCSD Department of Computer Science & Engineering
Computer Architecture from 10,000 feet

foo(int x) {
   ..
}

Class of application

Physics
In the olden days:

“In 1942, just after the United States entered World War II, hundreds of women were employed around the country as computers…” (source: IEEE)
The Great Battles in Computer Architecture Are About How to Refine the Abstraction Layers

```c
foo(int x) { .. }
```

**Computation**

- Language
- Compiler
- ISA
- Micro Architecture
- Register-Transfer Level
- Circuits
- Devices
- Materials Science

**Physics**

- Fortran
- IBM 360, VLIW
- RISC, T’meta
- Superscalar, caches
- Mead & Conway
Abstractions protect us from change -- but must also change as the world changes.

Changes in fabrication capabilities

Computation

Language
Compiler
ISA
Micro Architecture
Register-Transfer Level
Circuits
Devices

Materials Science

Slower Wires!
Denser VLSI gates!
More pins!
More Power/cm^2!
Abstraction Layers - reflected in organization of research communities

Computation

Language
Compiler
ISA
Micro Architecture
Reg-Transfer Level
Circuits
Devices
Materials Science

Physics

International Symposium on Computer Architecture (ISCA)
High Performance Computer Architecture (HPCA)
Architectural Support for Programming Languages and OS (ASPLOS)
International Symposium on Microarchitecture (MICRO)
Design Automation Conference (DAC)
Int. Conf. Computer Aided Design (ICCAD)
International Solid State Circuit Conference (ISSCC)
International Electron Devices Meeting (IEDM)
Classic ISSCC (Circuits) Paper: “How we designed a chip and how fast / low power it is.”
Classic Int. Electron Device Meeting (IEDM)

Paper: How we designed a single transistor

90 nm Generation Transistor

Nickel Silicide Layer
Silicon Gate Electrode
1.2 nm SiO₂ Gate Oxide
Strained Silicon

No other company combines these transistor features at the 90 nm generation.

Figure 11: 1.2 nm gate oxide time to fail vs. electric field.

Figure 6: NMOS I_on vs. I_off at 1.0V and 1.2V.
Classic Int. Electron Device Meeting (IEDM)
Paper: “How we designed a wire”

90 nm Generation Interconnects

Low-k CDO Dielectric

Copper Interconnects

Combination of copper + low-k dielectric now meeting performance and manufacturing goals

Intel
The focus of this class

- Language
- Compiler
- ISA
- Micro Architecture
- Reg-Transfer Level
- Circuits
- Devices
- Materials Science

- International Symposium on Computer Architecture (ISCA)
- High Performance Computer Architecture (HPCA)
- Architectural Support for Programming Languages and OS (ASPLOS)
- International Symposium on Microarchitecture (MICRO)
- Design Automation Conference (DAC)
- Int. Conf. Computer Aided Design (ICCAD)
- International Solid State Circuit Conference (ISSCC)
- International Electron Devices Meeting (IEDM)
Since technology change is such a big influence in architecture, and because it takes 3-6 years to create a totally new design, we try to predict & exploit it (with varying degrees of success.)
Moore's Law: 2X transistors / "year"

"Cramming More Components onto Integrated Circuits"
- Gordon Moore, Electronics, 1965

# on transistors / cost-effective integrated circuit double every N months (12 ≤ N ≤ 24)

Adapted from Patterson, CSE 252 Sp06 Lecture 2 © 2006 UC Berkeley.
One Important Change: Power
Santa Clara, we have a problem

More pipeline stages, less efficient, more power.

Just can’t remove
> 100 watts
without great expense on a desktop.

All computing is now
Low Power Computing!
Power Density

Power doubles every 4 years
5-year projection: 200W total, 125 W/cm²!

P=VI: 75W @ 1.5V = 50 A!

Change: microprocessor frequency versus time

- 5 yr / 10x (58%)
- 7 yr / 10x (39%)
- Power Limited

Faster Circuits,
Faster + Smaller Transistors,
Fast Microarchitecture

- Intel x86
Intel

P3: 12 stages
P4 (b4 paper): 20 stages
P4/prescott: 31 stages
P5/Tejas: >> 31 stages
Intel

P3: 12 stages
P4 (b4 paper): 20 stages
P4/prescott: 31 stages
P5/Tejas: >> 31 stages
Intel

P3: 12 stages
P4 (b4 paper): 20 stages
P4/prescott: 31 stages
P5/Tejas: >> 31 stages
Back to the future

P3:
12 stages

P4 (b4 paper):
20 stages

P4/prescott:
31 stages

P5/Tejas:
>> 31 stages

Same as 1996 – I can’t sell that. I must call it something new --- Pentium...Mmmm... Great Scott, I’ve got it!
And forward to multi-core

Intel Core Duo
Future outlook

Old Trend: Frequency

New Trend: Parallel processing
  → Intel is pushing multi-core instead of higher clocks (will we ever hit 10 GHz?)
  → good time to know something about architecture
  → your application may be feasible only if you can use the architecture efficiently
Abstractions protect us from change -- but must also change as the world changes

Changes in application space

- Language
- Compiler
- ISA
- Micro Architecture
- Register-Transfer Level
- Circuits
- Devices
- Materials Science

Virtual Homicide (Quake)
Photographic memory
Telepathic
Mathematical Genius
Etc...

Physics
And on that note: PC’s are not the only important class of computer - in fact they are in the minority (~2%)!
Administrative Details

***************
Course Work and Grading

- Let's Review the Course Website ...
Patterson & Hennessy, 4th revised edition of “Computer Organization, the Hardware/Software Interface”

- Decent book. We’ll read most of it.
  * not using 5th Edition, came out this year, look for errata
- Patterson is professor at Berkeley;
  * lead RISC project (foundation of SPARC processor)
  * lead RAID (redundant array of inexpensive disks) project
- Hennessy is professor at Stanford
  * now President of Stanford
  * co-founded of MIPS Computer Systems
- Note: same authors wrote the graduate textbook, “Computer Architecture, A Quantitative Approach”. 
Assigned readings for each lecture posted on website!

- Lectures will include material not in the text…text will include material not in the lectures.

- Resource limitations prevent us from addressing material from the prerequisites in office hours…but we are happy to refer you to the book or your classmates.
How to find out your deliverables

• Check the website. Generally, we won’t necessarily announce readings or assignment due dates in lecture.

http://www-cse.ucsd.edu/classes/ /cse141/

  e.g. www-cse.ucsd.edu/classes/fa12/cse141

• You will have assigned reading for every lecture except when you have an exam.

Please watch the website for course updates, reading assignments and homework assignments!
Who to ask which Question

Me:
“In lecture, …”
“I’m designing my own supercomputer, and…”

141 TA or Tutor:
“On problem 5, …”

141L TA or Tutor:
“In the Altera environment, … “

Me+141 TA or Tutor:
“In a 2-way set associative cache…”
“In the book, …”

Prof. Eldon, 141L TA or Tutor:
“In my 141L Implementation, …”

.. and of course, talk with your classmates!!
Am I Qualified to Teach You?

• PhD, MIT, EE & CS
  - ten years at MIT studying processor design
  - 8 years consulting for chip companies
  - various research publications

Architectures designed: 4
Machines Implemented: 3
Millions of units of software shipped: > 1
Million-gate chips designed: 2
Supercomputers designed: 1
About Me

PowerMush 3
PowerMush IV

Apple®

Virtual PC

mitraw

UCSD
About Me

~120 million transistors