CSE141 Winter 2014

Discussion Section 2: Single Cycle Datapaths and Control Signals
The Single Cycle CPU
Operation Sequence

1. Fetch - Obtain the next instruction
2. Decode - Find the opcode, parse instruction
3. Read Registers - Get register values from RF
4. Execute - Execute instruction (ALU/MEM)
5. Write Register - Write into the RF
6. Update
   a. If branching set PC to branch + offset
   b. If not branching PC = PC +4
Control Signals
Ex.1 Control Signals (Add)

ALUsrc
ALUop
MemWrite
MemToReg
RegDst
RegWrite
MemRead

Shelby Thomas
Ex.1 Control Signals (Add)

ALUsrc = 1
ALUop = ADD
MemWrite = 0
MemToReg = 0
RegDst = 0
RegWrite = 1
MemRead = 0
Ex.2 Control Signals (LW)

ALUsrc
ALUop
MemWrite
MemToReg
RegDst
RegWrite
MemRead

Shelby Thomas
Ex.2 Control Signals (LW)

- ALUsrc = 1
- ALUop = ADD
- MemWrite = 0
- MemToReg = 1
- RegDst = 0
- RegWrite = 1
- MemRead = 1
Ex.3 Control Signals (SW)

ALUsrc
ALUop
MemWrite
MemToReg
RegDst
RegWrite
MemRead
**Ex.3 Control Signals (SW)**

- ALUsrc = 1
- ALUop = SW
- MemWrite = 1
- MemToReg = x
- RegDst = x
- RegWrite = 0
- MemRead = 0
### Ex. Control Signal Matrix

<table>
<thead>
<tr>
<th>Operation</th>
<th>RegDst</th>
<th>RegWrite</th>
<th>ALUSrc</th>
<th>ALUOp</th>
<th>MemWrite</th>
<th>MemRead</th>
<th>MemToReg</th>
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<tbody>
<tr>
<td>add</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>010</td>
<td>0</td>
<td>0</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>110</td>
<td>0</td>
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<td>0</td>
</tr>
<tr>
<td>and</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>000</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>or</td>
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<td>001</td>
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<td>0</td>
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<tr>
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<td>1</td>
<td>0</td>
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<td>1</td>
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<tr>
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<td>X</td>
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<td>110</td>
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<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>